(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

CORRECTED VERSION

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 September 2001 (20.09.2001)

PCT

(10) International Publication Number
WO 2001/069328 A3

(51) International Patent Classification?: G04F 10/00

(21) International Application Number: PCT/CA2001/000364

(22) International Filing Date: 16 March 2001 (16.03.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/189,975 17 March 2000 (17.03.2000) US

(71) Applicant (*for all designated States except US*): VECTOR 12 CORPORATION [US/CA]; Suite 2143, 13358 Commerce Parkway, Richmond, British Columbia V6V 3A1 (CA).

(72) Inventors; and

(75) Inventors/Applicants (*for US only*): TABATABAEI, Sassan [IR/CA]; 313 - 809 West 16th Street, North Vancouver, British Columbia V7P 1R2 (CA). IVANOV, Andre [CA/CA]; 10591 Yarnish Drive, Richmond, British Columbia V7E 5H6 (CA).

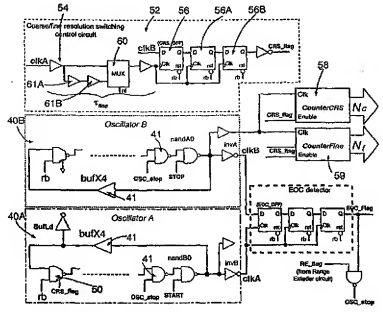
(74) Agent: MANNING, Gavin, N.; Oyen Wiggs Green & Mutala, 480 - 601 West Cordova Street, Vancouver, British Columbia V6B 1G1 (CA).

(81) Designated States (*national*): AE, AG, AL, AM, AT (utility model), AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ (utility model), CZ, DE (utility model), DE, DK (utility model), DK, DM, DZ, EE (utility model), EE, ES, FI (utility model), FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK (utility model), SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE,

[Continued on next page]

(54) Title: HIGH RESOLUTION TIME-TO-DIGITAL CONVERTER



(57) Abstract: A time to digital converter (TDC) has a pair of digital oscillators. The periods of the oscillators differ by T_Δ. The oscillators are triggered by START and STOP pulses. A counter counts a number of pulses until reference points on the signals output by the oscillators coincide. Measurements may be made using a dual resolution method. Intrinsic jitter of the TDC can be determined by comparing sets of measurements in which the switch in resolutions is made at different points.

WO 2001/069328 A3

IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(88) Date of publication of the international search report:
22 August 2002

(48) Date of publication of this corrected version:
15 April 2004

(15) Information about Correction:
see PCT Gazette No. 16/2004 of 15 April 2004, Section II

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 September 2001 (20.09.2001)

PCT

(10) International Publication Number
WO 01/69328 A2

(51) International Patent Classification⁷: G04F 10/00

(21) International Application Number: PCT/CA01/00364

(22) International Filing Date: 16 March 2001 (16.03.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/189,975 17 March 2000 (17.03.2000) US

(71) Applicant *(for all designated States except US)*: **VECTOR 12 CORPORATION** [US/CA]; Suite 2143, 13358 Commerce Parkway, Richmond, British Columbia V6V 3A1 (CA).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **TABATABAEI, Sassan** [IR/CA]; 313 - 809 West 16th Street, North Vancouver, British Columbia V7P 1R2 (CA). **IVANOV, Andre** [CA/CA]; 10591 Yarmish Drive, Richmond, British Columbia V7E 5E6 (CA).

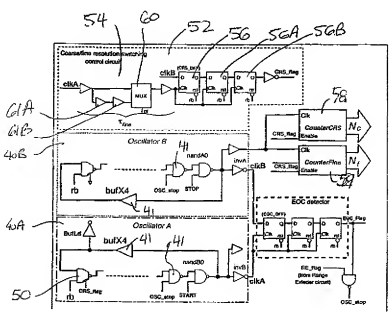
(74) Agent: **MANNING, Gavin, N.**; Oyen Wiggs Green & Mutala, 480 - 601 West Cordova Street, Vancouver, British Columbia V6B 1G1 (CA).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AT (utility model), AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, CZ (utility model), DE, DE (utility model), DK, DK (utility model), DM, DZ, EE, EE (utility model), ES, FI, FI (utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (utility model), SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: HIGH RESOLUTION TIME-TO-DIGITAL CONVERTER



(57) Abstract: A time to digital converter (TDC) has a pair of digital oscillators. The periods of the oscillators differ by T_Δ. The oscillators are triggered by START and STOP pulses. A counter counts a number of pulses until reference points on the signals output by the oscillators coincide. Measurements may be made using a dual resolution method. Intrinsic jitter of the TDC can be determined by comparing sets of measurements in which the switch in resolutions is made at different points.

WO 01/69328 A2

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

HIGH RESOLUTION TIME-TO-DIGITAL CONVERTER

Cross-Reference to Related Application

[1] This application claims the benefit of the filing date of U.S. application No. 60/189,975 filed on 17 March, 2000, which is hereby incorporated by reference in its entirety.

Technical Field

[2] This invention relates to time-to-digital conversion ("TDC"), more specifically to time to digital conversion methods and apparatus which use a differential delay between frequency-mismatched oscillators to measure time between events to high resolution. The invention has particular application in measuring jitter characteristics in high frequency digital signals. Specific embodiments of the invention are useful for on board self testing of timing circuits such as phase-locked loops ("PLLs"), delay-locked loops ("DLLs"), and serialiser/deserializers. Another aspect of the invention relates to a finely tunable digital ring oscillator suitable for use in TDC systems according to the invention.

Background of the Invention

[3] Jitter is an important characteristic of high-speed digital signals generally. While there exist sophisticated stand-alone devices capable of measuring jitter in high-speed digital signals, such devices tend to be extremely complicated and expensive. Jitter testing typically requires a long test time. Further, where the signal to be tested is internal to an integrated circuit, it may not be practical to use a stand-alone device to test for jitter.

[4] Timing circuits such as phase-locked loops, delay-locked loops, and serializers/deserializers are used widely in many high-speed integrated circuits. These circuits are used in many applications. Some examples are synthesizing clock signals, recovering data, realigning clock edges and timing the transmission of data.

[5] Jitter in the outputs of such timing circuits can cause malfunctions. These malfunctions can be very difficult to diagnose. As complex System on Chip ("SOC") integrated circuits become even more complicated and clock speeds increase into the gigahertz range, it becomes increasingly costly and time consuming to test such circuits.

[6] The definition of jitter varies depending on the field of application. In sequential circuits, e.g. CPUs, jitter is defined as the variation of the clock period, known as "cycle-to-cycle" or "period jitter". Such variation is best modelled as a frequency modulation of the clock signal. More formally period jitter can be expressed as:

$$V_{FM}(t) = sgn[\sin\left(\int_0^t \frac{2\pi}{T_0 + T_j(t)} dt\right)] \quad (1)$$

where V_{FM} is the clock signal, T_0 is the average clock period, $T_J(t)$ is the frequency modulating jitter signal, and sgn[x] is the sign function:

$$sgn[x] = \begin{pmatrix} 1 & x>0 \\ 0 & x\leq 0 \end{pmatrix} \quad (2)$$

As shown in Figure 1A, period jitter samples are collected by measuring the duration of each period of the signal IN1.

[7] For both period and accumulative jitter measurements, *M* jitter samples are collected to calculate jitter characteristics, such as rms, peak-to-peak, or frequency components. For example, the rms jitter may be obtained by performing the following computations:

$$T_{J(rms)} = \sqrt{\frac{1}{M}\sum_{i=0}^{M-1} T_J^2(i)} \qquad - 3 -$$

[8] The important jitter specifications for PLLs used in digital communication interfaces are intrinsic jitter, jitter tolerance and jitter transfer. These specifications are given in standards for each application (e.g., see Bell Research Laboratories *SONET transport systems: Common criteria network element architectural features* GR-253 core, Issue 1, pp. 5-81, December, 1994 for SONET interfaces).

[9] Intrinsic jitter is defined as the jitter at the output of the PLL when the input is jitter-free. This is often expressed in terms of unit interval **UI**, which is defined as the period of a signal with a frequency equal to the average frequency of the original signal. For example in a 155.54 MHz SONET network application, 1 **UI** is 6.429 ns.

[10] Jitter transfer is defined as the ratio of the output jitter to input jitter of the PLL as a function of frequency.

[11] Jitter tolerance is the peak-to-peak amplitude of the sinusoidal jitter applied to the input of the PLL which causes 1dB power penalty (in terms of bit error rate).

[12] There is a need for systems capable of measuring jitter characteristics of high-speed digital signals. There is a particular need for such systems capable of measuring jitter in timing circuits internal to complicated integrated circuits.

[13] Functional testing is typically the only practical way to test today's high-speed timing circuits. Most structural test methods are too intrusive (i.e. the testing itself has a significant effect on the performance of the circuit) or provide poor correlation to important specifications such as jitter. Jitter specifications are typically the single most important set of specifications for a high-speed timing circuit. Jitter specifications include intrinsic jitter, jitter transfer functions and jitter tolerance. Testing such a circuit to determine whether its actual jitter characteristics meet its specifications is a significant problem.

[14] Various authors have proposed methods for testing devices such as PLLs. All of these proposed methods have disadvantages. R.J.A. Harvey et al. *Test evaluation for complex mixed-signal IC's by introducing layout dependent faults*, IEEE Colloquium on Mixed Signal VLSI Test, pp. 6/1-8, 1993 suggests testing PLLs by performing partial specification testing by measuring lock range, lock time and power supply current. Dalmia et al. *Power supply current monitoring techniques for testing PLLs* Proc. of Asian Test Symposium, pp. 366-371, 1997 and Dalmia et al., U.S. patent No. 5,835,501 disclose the use of power supply current monitoring for PLL testing.

[15] Devarayanadurg et al. *Hierarchy based statistical fault simulation of mixed signal IC's* Int. Test Conf. pp. 521-527, 1996 and Goteti et al. *DFT for embedded charge-*

pump PLL systems incorporating IEEE 1149.1, Proc. of Custom Integrated Circuits Conf. pp. 210-213, 1997 propose methods for efficient fault simulation of PLLs and suggest lock frequency range measurement for PLL testing.

[16] Although a combination of these techniques seems to provide a good efficient fault simulation it is difficult to correlate the test results to important jitter specifications. This is partly because simulating jitter for fault-free and faulty circuits is extremely difficult due to a lack of tools capable of simulating noise in non-linear dynamic circuits.

[17] Azias et al. *A unified digital test technique for PLLs using reconfigurable VCO* Proc. of Int. Mixed Signal Test Workshop, 1999 discloses a reconfiguration technique for testing ring oscillator-based PLLs. This technique has the advantage of being compatible with digital test methods, but it requires reconfiguring sensitive parts of a PLL. Also, it exhibits the problem of unknown correlation of test results and functional specifications.

[18] S. Sunter et al. *BIST for phase-locked loops in digital applications*, Proc. of Int. Test Conf. pp. 532-540, 1999 discloses a BIST circuit capable of measuring lock range and loop gain of a PLL in addition to performing a jitter test. Methods which use this circuit to measure jitter depend on bit error rate (BER) and so can only provide statistical information about jitter. Such methods may give pessimistic estimates of jitter in noisy digital environments. This might lead to discarding some good devices. The jitter testing approach of Sunter et al. is limited primarily to clock recovery PLLs.

[19] US patent Nos. 5,663,991 and 5,889,435 disclose on-chip jitter measurement techniques for testing PLL circuits. The BIST circuits proposed in these patents are mixed-signal and their resolution is limited to one gate delay. This is inadequate for testing high-speed PLLs.

[20] Veillette et al. *On-chip measurement of the jitter transfer function of charge-pump phase locked loops*, Int. Test Conf. pp. 776-785, 1997 disclose a jitter transfer function measurement circuit. This circuit does not have sufficient resolution for intrinsic jitter testing.

[21] Veillette et al., *Stimulus generation for built in self test of charge pumped phase locked loops*, Int. Test Conf. pp. 698-707, 1998 proposes a method for generating jitter at the input of a PLL for jitter transfer testing. This method, however, requires reconfiguration of the feedback in the PLL loop, which could affect the performance of the loop.

[22] Another on-chip jitter test method is to determine jitter by measuring time intervals between the significant edges of one or two signals. Such measurement can be done with a time-to-digital converter (TDC). A TDC produces a digital output representing the time elapsed between two temporally separated events. Figures 1A, 1B and 1C illustrate respectively how period, accumulative jitter, and relative jitter can be measured through the use of a TDC 10.

[23] Various TDC circuits have been used in physics experiments. It has been suggested that such TDC circuits could be used in jitter measurement. Existing TDC circuits are, however, mixed-signal, require custom design and layout, occupy large areas, do not provide

high resolution, or rely heavily on matching of the elements.

[24] Kelkar et al. U.S. patent No. 5,663,991 discloses the use of a controlled delay line in an on-chip jitter measurement method. This circuit is mixed-signal and suffers from the same limitations as most TDCs.

[25] In serial communication applications, jitter can be defined as the short-term variations of a digital signal's significant instants, e.g. rising edges, from their ideal position in time. Such jitter is often denoted as "accumulative jitter" and is described as a phase modulation of a clock signal. In a clock synthesis circuit, where the absolute jitter is important, often a jitter-free (practically low-jitter) reference signal is used for jitter measurement. In such a case, the difference between the position of corresponding edges of the signal (IN1) relative to the reference clock (REF) indicates the jitter. Figure 1B illustrates how accumulative jitter samples, $\tau_{j(i)}$ for i=1,...,N can be collected using a TDC.

[26] Sometimes, the relative jitter between two signals is of interest if neither of the two signals is a jitter-free signal, e.g. in data recovery circuits. Fig. 1C shows how relative jitter between the edges of signal IN1 and IN2 can be measured using a TDC.

[27] A classic method of measuring a time interval is to start a counter at the beginning of the interval and stop it when the interval ends. The resulting number in the counter will be proportional to the time interval. The resolution in this method is the period of the clock controlling the counter. To measure intrinsic jitter of a high-speed PLL (e.g. a 155MHz clock synthesis PLL), where a high resolution in the range of 20 ps is required, a

clock frequency of 50 GHZ would be needed. This method is not suitable for on-chip applications where the maximum clock available is in the range of a few hundreds of MHz.

[28] Santos, *A CMOS delay locked and sub-nanosecond time-to-digital converter chip*, IEEE trans on nuclear science, vol. 43, pp. 1717-1719, June, 1996 discloses a TDC based on the use of a delay chain. In this circuit, the output of the delay elements in the delay chain are set HIGH as the START rising edge travels through them. A delay locked loop (DLL) is used to calibrate the delay elements to a known delay. Such a calibration requires very good matching between all the delay elements in both the delay chain and the DLL.

[29] Arai, *A time digitizer CMOS gate array with a 250 ps time resolution*, IEEE Journal of Solid-State Circuits, v. 31, pp. 212-220, February, 1996 discloses an alternative TDC in which an analog delay chain and DLL are combined. This obviates the need for element matching. In both of the schemes of Santos and Arai the DLL and the controlled delay elements are analog.

[30] A fully digital TDC could be made by eliminating the DLL and using digital gates as delay elements. The trade-off is decreased accuracy due to the quantization error associated with calibration reference inputs. The resolution T_s of such methods without time interpolation is limited to one gate delay at best. In current 0.35 µm CMOS technology, the smallest gate delay is approximately 50 ps, whereas a resolution and precision of about 20ps is required for functional testing of high-speed PLLs with 155 MHz center frequency. Also, since this delay is dependent on process variations and temperature, the resolution in such schemes is not controllable.

[31] Christiansen, *An integrated high resolution CMOS timing generator based on an array of delay locked loops*, IEEE Journal of Solid-State Circuits, v. 31, pp. 952-957, February, 1996 proposes the use of an array of DLLs to improve the measurement resolution. Mota et al. *A high resolution time interpolator based on a delay locked loop and an RC delay line*, IEEE Journal of Solid-State Circuits, v. 34, pp. 1360-1366, October, 1999 propose the use of an RC delay line to increase the measurement resolution through time interpolation. Although resolutions in the range of 25ps (rms) have been reported in these papers, the design of these circuit requires a great deal of care because of the need for a high degree of matching. Also, the design and layout of the DLL need careful attention due to the presence of significant power supply noise in large mixed-signal ICs.

[32] Kalisz et al., *Field programmable gate array based time to digital converter with 200 ps resolution*, IEEE Trans. on Instrumentation and Measurement, v. 46, pp. 51-55, February, 1997 propose a differential delay technique based on using two delay chains. One chain is composed of gates (each with a delay of τ_g. The other chain is made of latches (each with a delay of τ_l).In this technique the time quantization step is the difference between the delay of the delay elements in the two delay chains. A difficulty with this technique is that, since gates and latches are very different structures, τ_g and τ_l are likely to differ significantly. This makes it difficult to achieve high resolution (in the range of 20 ps or less).

[33] All the schemes mentioned above require good matching of the elements in the delay chains to achieve good accuracy. This is difficult to achieve within an

acceptable accuracy under typical process variations. As the time interval to be measured becomes longer, more elements must be added to the delay chains, making it even more difficult to assure matching of delays in the chains. When more elements more added the elements will have to be placed further apart and more routing delay will have to be accounted for. Therefore, these schemes make it difficult to provide acceptable TDC linearity. In addition, these schemes do not lend themselves well to automatic place and route. Furthermore, the resolution is set by the process parameters on each chip and cannot be controlled or adjusted.

- There is a need for a system capable of measuring directly the jitter characteristics of PLLs and other timing circuits on integrated circuit chips. Such a system should be:
- compact (i.e. small in area compared to the circuit under test ("CUT"));
- simple and quick to design;
- robust (i.e. resistant to process variations, temperature and power supply variations);
- provide a digital output (i.e. the system should generate one or more digital signatures which can be sent off-chip at relatively low speed, e.g. serially;
- accurate (measurement accuracy must be sufficient for the test);
- capable of being calibrated (i.e. the system should be calibration-free, self-calibrating, or use readily available signals to the chip for calibration); and,
- have little or no impact on the performance of the CUT.

Summary of the Invention

[34] One aspect of this invention provides a time to digital converter (TDC). The TDC comprises a timing circuit which includes first and second digital oscillators. The oscillators produce first and second clock signals respectively. The first and second oscillators have different periods. The invention uses the accurately known difference between the periods of the first and second oscillators to make high resolution time measurements. In preferred embodiments of the invention, at least one of the oscillators comprises a plurality of digitally controllable delay elements. The delay elements, when activated alter the period of the oscillator.

[35] The TDC also includes a coincidence detector connected to generate a coincidence signal when a reference point in the first clock signal has a known time relationship to a corresponding reference point on the second clock signal. In preferred embodiments of the invention the coincidence detector comprises a flip flop which is set when a rising edge of the first clock signal coincides with a corresponding rising edge of the second clock signal.

[36] A first counter is connected to count a number of cycles of the first oscillator until the coincidence detector generates the coincidence signal. The number is related to the length of an interval between starting the first oscillator and starting the second oscillator.

[37] A resolution adjustment circuit is connected to start the first and second oscillators at times separated by a known interval compare the number to a threshold and, if the number is not at least equal to a threshold

value altering the period of at least one of the oscillators by activating or deactivating one or more of the digitally controllable delay elements.

[38] In a preferred, dual resolution, embodiment the first and second oscillators are switchable between a first state wherein a difference in periods of the first and second signals is $T_{\Delta 1}$ and a second state wherein a difference in periods of the first and second signals is $T_{\Delta 2}$ where $T_{\Delta 2} < T_{\Delta 1}$; and the time to digital converter comprises a resolution switching control circuit connected to switch the timing circuit from its first state to its second state, a second counter connected to count a number of edges of the first signal between a START signal and a time when the timing circuit is switched from its first state to its second state, the first counter connected to count a number of edges of the first signal between the time when the timing circuit is switched from its first state to its second state and the time when coincidence signal is generated.

[39] Another aspect of the invention provides a time to digital converter comprising a timing circuit comprising first and second digital oscillators producing first and second clock signals respectively. The first and second oscillators are switchable between a first state wherein a difference in periods of the first and second signals is TΔ1 and a second state wherein a difference in periods of the first and second signals is TΔ2 where TΔ2 < TΔ1. A resolution switching control circuit is connected to switch the timing circuit from its first state to its second state when the reference point of the first clock signal approaches the known time relationship with the reference point of the second clock signal. A coincidence detector connected to generate a coincidence signal when a reference point in the first clock signal has a known

time relationship to a corresponding reference point on the second clock signal. A first counter is connected to count a number of edges of the first clock signal between the time when the timing circuit is switched from its first state to its second state and the time when the coincidence signal is generated and a second counter is connected to count a number of edges of the first signal between a START signal and a time when the timing circuit is switched from its first state to its second state.

[40] In a preferred embodiment of the invention, the resolution switching control circuit comprises a delay element connected to provide a delayed first clock signal and a coincidence detector connected to generate a coincidence signal when a reference point in the second clock signal has a known time relationship to a corresponding reference point on the delayed first clock signal. Most preferably the delay element has a first state resulting in a first delay of the delayed first clock signal and a second state resulting in a second delay of the delayed first clock signal different from the first delay.

[41] A further embodiment of the invention provides a digital timing circuit for generating first and second digital output signals having first and second periods. The timing circuit comprises a first ring oscillator triggered by a first control signal and generating a first clock signal; and a second ring oscillator triggered by a second control signal and generating a second control signal. At least one of the oscillators comprises a plurality of digitally controllable delay elements. The delay elements, when activated alter the period of the oscillator. The timing circuit comprises a coincidence detector connected to generate a coincidence

signal when a reference point in the first clock signal has a known time relationship to a corresponding reference point on the second clock signal. A counter is connected to count a number, *N*, of cycles of the first oscillator between the first control signal and the coincidence signal. A resolution adjustment circuit connected to generate the first and second control signals at times separated by a known interval, compare the number N to a threshold Nth and, if N is not at least equal to a threshold value altering the period of at least one of the oscillators by activating or deactivating one or more of the digitally controllable delay elements.

[42] A still further aspect of the invention provides a method for producing first and second digital signals having first and second periods. The method comprises providing a pair of digital oscillators; starting the first oscillator and starting the second oscillator a time period Td after starting the first oscillator; counting a number N of cycles of the first oscillator until a reference point on the first signal coincides with a corresponding reference point on the second signal; if N is not at least equal to a threshold value altering the period of at least one of the oscillators and repeating these steps until N is at least equal to the threshold value.

[43] In preferred embodiments of the invention, varying a period of at least one of the oscillators comprises changing a state of a controllable delay element.

[44] A yet further aspect of the invention provides a method for time to digital conversion comprising providing first and second digital oscillators having

periods which differ by an amount T_Δ wherein the first and second oscillators are switchable between a first state wherein a difference in periods of the first and second signals is $T_{\Delta 1}$ and a second state wherein a difference in periods of the first and second signals is $T_{\Delta 2}$ where $T_{\Delta 2} < T_{\Delta 1}$; starting the first oscillator upon the occurrence of a first control signal and starting the second oscillator on the occurrence of a second control signal a time T_d later; when the reference points occur within a known time delay of one another switching the oscillators to their second state; counting a number N_c of edges of the first clock signal which occur between the first control signal and a time when the oscillators are switched to their second state; and, counting a number N_F of edges of the first clock signal which occur between the time when the oscillators are switched to their second state and a time when the reference points have a known time relationship.

[45] The method may include estimating a noise floor for the first and second oscillators by acquiring a first set of the numbers N_F and N_c for T_d having a known value Tref while the known time delay has a first value and a second set of the numbers N_F and N_c for T_d having a known value Tref, or a known multiple of T_{ref}, while the known time delay has a second value, averaging N_F and N_c for each set of measurements and computing the noise floor from the average values of N_F and N_c for the two sets of measurements.

[46] Another aspect of the invention provides a frequency tunable digital ring oscillator comprising a closed signal path defined at least in part by a plurality of series connected delay elements each having an input and an output the delay elements comprising at least one digitally controllable delay element. The

digitally controllable delay element comprises a gate connected in series with the signal path and a tri-state device having an input connected to an output of the gate and a control connection connected to a control device.

[47] The tri-state device may be a tri-NOT gate or a tri-state buffer, for example.

[48] Further features and advantages of the invention are described below.

Brief Description of the Drawings

[49] In figures which illustrate non-limiting embodiments of the invention:

Figures 1A, 1B and 1C are schematic block diagrams which illustrate respectively how period, accumulative jitter, and relative jitter can be measured through the use of a TDC;

Figure 2 is a block diagram illustrating major components of a jitter measurement circuit according to the invention;

Figure 3 is a block diagram of a TDC circuit according to the invention;

Figure 4A is a schematic circuit diagram of a simple single resolution time quantizer according to the invention;

Figure 4B illustrates waveforms of digital signals at various locations in the time quantizer of Fig. 4A;

Figure 5A is a schematic circuit diagram of a dual resolution time quantizer according to the invention;

Figure 5B illustrates waveforms of digital signals at various locations in the time quantizer of Fig. 5A;

Figure 6A is a schematic circuit diagram of a range extender circuit;

Figure 6B illustrates waveforms of digital signals at various locations in the range extender circuit of Fig. 6A;

Figure 7A is a schematic circuit diagram of an alternative range extender circuit;

Figure 7B illustrates waveforms of digital signals at various locations in the range extender circuit of Fig. 7A;

Figure 8 is a schematic diagram of an automatic resolution adjustment circuit;

Figure 9A is a TATB checker circuit;

Figures 9B and 9C are waveforms at locations in the circuit of Figure 9A for $T_A > T_B$ and $T_A < T_B$ respectively;

Figure 10A is an alternative TATB checker circuit;

Figure 10B illustrates waveforms of digital signals at various locations in the TATB checker circuit of Fig. 10A;

Figure 11A is a flow chart illustrating an exhaustive search method for tuning a pair of oscillators to have a small period difference where controllable delay elements in the oscillators have fixed steps;

Figure 11B is a flow chart illustrating a directed search method for tuning a pair of oscillators to have a small period difference where controllable delay elements in the oscillators have fixed steps;

Figure 12 is a flow chart illustrating an exhaustive search method for tuning a pair of oscillators to have a small period difference where controllable delay elements in the oscillators have incrementally varying steps;

Figure 13 is a flow chart illustrating a semi-exhaustive search method for tuning a pair of oscillators to have a small period difference where controllable delay elements in the oscillators have incrementally varying steps;

Figure 14 is a flow chart illustrating a fast search method for tuning a pair of oscillators to have a small period difference where controllable delay elements in the oscillators have incrementally varying steps;

Figures 15A through 15E are schematic diagrams illustrating various types of load elements and their simplified models;

Figure 16 is a schematic diagram of a circuit for testing the effect of control voltage variations on time delay provided by a controllable delay element;

Figures 17A and 17B are schematic diagrams of controllable delay elements based on a multiplexer;

Figures 18A, 18B and 18C are schematic views of controllable delay elements in which a variable load is applied by the input of a tri-state device;

Figures 19A and 19B are schematic diagrams illustrating the structure of typical tri-NOT gates;

Figures 20A, 20B and 20C are schematic views of controllable delay elements having tri-state devices connected in parallel with other gates;

Figure 21 is a schematic view of a selection circuit for providing a reference interval;

Figure 22 is a schematic view of a jitter generator circuit;

Figure 23 is a schematic view of a configuration of edge sample suitable for cycle-to-cycle jitter measurement;

Figure 24A is a schematic view of a configuration of edge sample suitable for relative jitter measurement;

Figure 24B is a timing diagram illustrating significant signals in the circuit of Figure 24A;

Figure 25 is a top level diagram of various components in an example embodiment of a jitter measurement system according to the invention;

Figure 26 is a schematic diagram of the time quantizer circuit of the jitter measurement system of Figure 25;

Figure 27 is schematic diagram of the RE_TAB block of Figure 25;

Figures 28 and 29 are schematic diagrams of 3-bit and 6-bit comparators used in the RE_TAB block of Figure 27;

Figure 30 is a schematic view of a calibration interval generator circuit of the jitter measurement system of Figure 25;

Figure 31 is a schematic view of a TATB checker circuit for the jitter measurement system of Figure 25; and,

Figure 32 is a timing diagram for some signals present during a TATB check and resolution adjustment process.

List of Reference Numerals

20	circuit	22	time-to-digital converter
24	edge sampler	26	edge sampler controller
30, 30A 30B	time quantizer	32	resolution adjustment block
34	range extender block	34A 34B	range extender circuit
36	calibration circuit	38	TDC controller
40, 40A 40B	oscillators	41, 41A	delay elements
42	coincidence detector	43A	circuit
44, 44A, 44B	flip flop	46	counter

48	NAND gate	50	delay element
52	resolution control circuit	54	delay line
56, 56A 56B	flip flop	58	counter
59	counter	60	multiplexer
61	delay elements	70A 70B	counters
71	pulse	72	comparator
73	flip flop	74A 74B	flip flops
75	gate	76A, 76B 76C, 76D	delay elements
77A 77B	glitch	78A 78B	flip flops
79	pulse	82	resolution adjustment controller
84, 84A, 84B	TATB circuit checker	85, 86	flip flops
88	counter	89	gate
90A, 90B	counter	92	comparator
93, 94	flip flops	100A	method
100B	method	110	method
112A, 112B 112C, 112D 112E	load element	113	capacitance
114	switch	115A 115B	delay elements
116	multiplexer	117A	delay element
119	logic gate	120	tri-state NOT-gate

122	delay element	123	NOT-gate
124	tri-NOT gate	130	circuit
132, 133	flip flop	134	K_DGen state machine block
140	circuit	141	delay line
142	multiplexer	143	sequence counter
150	edge sampler circuit	151, 152	flip flop
153	delay element		

Description

[1] In this description, a variable denoted by t refers to an instant in time, T refers to a time interval, and τ refers to a time delay associated with the operation of a physical structure, such as a gate or a latch. In this description the following notation is used:

- t_{START} - the time of the START event (typically this is the time when the START signal is set HIGH);
- t_{STOP} - the time of the STOP event (typically this is the time when the STOP signal is set HIGH);
- $T_d = t_{STOP} - t_{START}$ the time interval to be measured;
- clkA the output signal produced by oscillator 40A;
- clkB the output signal produced by oscillator 40B;
- T_A - the period of clkA;
- T_B - the period of clkB;
- $t_{X(i)}$ - the time at which the i^{th} rising edge of clkX (X=A or B) occurs;
- $T_d = T_A - T_B$ the time quantization step;
- N - a value generated by the time quantizer 30 from which T_d can be determined;
- M_A - the output state of counter CntrA; and,

- M_B - the output state of counter CntrB.

[2] This invention provides digital circuits which are capable of measuring jitter in digital signals with high resolution. The circuits may be used to measure jitter characteristics of PLLs and may also be used to measure jitter in other signals. Figure 2 shows a digital circuit 20 according to the invention. Circuit 20 includes a high-resolution time-to-digital converter 22. TDC 22 measures the duration of a time interval T_d between a start event and a stop event. In the illustrated embodiment of the invention an edge sampler 24 generates the start and stop events. The start and stop events may respectively be, for example, rising edges of START and STOP signals. Edge sampler 24 is controlled by an edge sampler controller 26.

[3] Under the control of edge sampler controller 26, edge sampler 24 selects the appropriate START and STOP edges and passes them to TDC 22. Edge sampler 24 and edge sampler controller 26 can preferably be configured for measuring various jitter specifications as described in more detail below.

[4] Figure 3 illustrates a circuitry for one embodiment of TDC 22 suitable for use in this invention. TDC 22 includes a time quantizer 30 which quantizes time with a time resolution of T_Δ. A resolution adjustment block 32 controls T_Δ to be less than a programmable threshold. A range extender block 34 extends the maximum time interval that time quantizer 30 is capable of measuring. A calibration circuit 36 is used to obtain a precise estimate of T_Δ with reference to a low-jitter reference clock. A TDC controller 38 controls the overall operation of TDC 22.

[5] Initially the resolution of time quantizer 30 is adjusted by resolution adjustment block 32 and time quantizer is calibrated. Then edge sampler controller 26 causes edge sampler 24 to generate START and STOP signals for a signal of interest and to pass pairs of START and STOP signals as jitter samples to time quantizer 30 for measurement. Time quantizer 30 measures values related to the intervals between the START and STOP signals. These measured values can be used to determine jitter characteristics of the signal of interest, as described below.

[6] A simple single resolution time quantizer 30A is shown in Figure 4A. Time quantizer 30 may be constructed to provide multiple, preferably two, different resolutions. Figure 5A shows a time quantizer 30B which provides coarse and fine resolutions. Referring to Figure 4A, time quantizer 30A includes a pair of oscillators 40A and 40B (generally oscillators 40). Each oscillator 40 comprises a closed signal path along which a plurality of delay elements 41 are connected in series. Oscillators 40A and 40B have slightly different periods. Time quantizer 30 uses a differential method to obtain high resolution. This reduces the need for circuit matching.

[7] The time quantizer 30A of Figure 4A comprises oscillators 40, a coincidence detector 42 (in the illustrated embodiment, coincidence detector 42 comprises a flip flop 44) and a counter 46. The resolution of time quantizer 30A is determined by T_d. The periods of oscillators 40A and 40B are set to be very slightly different so that T_d is a short time. T_d may be, for example, about 20 ps. T_A is slightly larger than T_B.

[8] Figure illustrates waveforms involved in the operation of time quantizer 30A. Oscillators 40A and 40B

start oscillating on the rising edges of START and STOP respectively. Counter 46 starts counting on the rising edge of STOP. Coincidence detector 42 determines when reference points on the waveforms of clkA and clkB are in a known temporal relationship. In the illustrated embodiment the reference points are the rising edges of clkA and clkB. Flip flop 44 samples clkB at the rising edge of clkA. If flip flop 44 detects that clkB has a value of HIGH then flip flop 44 sets EOC_flag. Assuming that T_d is larger than T_Δ, EOC_flag will be low for the first cycle of clkB. However, in each successive cycle of clkB, the rising edge of clkB gets closer to the corresponding rising edge of clkA by an amount T_Δ. Eventually the N-th rising edge of clkB will precede the corresponding rising edge of clkA by at least the setup time of flip flop 44. When this occurs, EOC_flag changes state.

[9] When EOC_flag changes state, the value in counter 46 is preserved. In the illustrated example oscillators 40 stop oscillating and counter 46 stops counting when EOC_flag is set HIGH. The value N in counter 46 indicates the value of T_d. In preferred embodiments, EOC_flag also initiates processing of data and prepares TDC 20 to measure another time interval.

[10] Preferably coincidence detector 42 is constructed to avoid logic errors which might be caused by metastable behaviour of flip flop 44. Metastable behaviour may occur if, for some value of T_d, the interval between corresponding rising edges of clkA and clkB is within the metastability window of flip flop 44. Under these circumstances it may take significantly longer than $\tau_{CLK\text{-}to\text{-}Q}$ for the output EOC_DFF to switch to its HIGH state. If counter were driven directly by the EOC_DFF signal output

by flip flop 44 then this could cause an unknown clock state for counter 46.

[11] In the illustrated embodiment, coincidence detector 42 comprises a triple flip flop synchronizer comprising flip flops 44, 44A and 44B. The output of flip flop 44B provides the EOC_flag signal. In this embodiment, if metastable behaviour of flip flop 44 prevents EOC_DFF from settling to its HIGH value after the *Nth* rising edge of clkB then the decision to end the measurement will be made at the *N+1th* rising edge of clkB. This is because the relative delay between the *N+1th* edges of clkA and clkB is greater than the delay between the *Nth* edges of clkA and clkB by T_Δ, which is much greater than the metastability window of flip flop 44. For example, the metastability window of flip flops in some 0.35 μm CMOS digital cell libraries is less than 0.01 ps. Since the metastability window of flip flop 44 is typically extremely short, it will not significantly affect the precision with which jitter can be measured.

[12] It can be shown that the value N in counter 46 at the end of conversion is related to T_d as follows:

$$NT_\Delta = T_d + T_C + T_Q + T_R \qquad (4)$$

where T_C is a constant offset time, T_Q is the quantization error ($0 \le T_Q < T_\Delta$), and T_R is a random error due to intrinsic jitter of gates, flip flops and other components of TDC 20.

[13] Completing one measurement takes some time. The amount of time required for each measurement depends upon the value of T_Δ. If the error term of Equation (4) is negligible then the time T_{meas} required for one measurement can be shown to be:

$$T_{meas} = NT_A = \frac{T_d + T_C}{T_\Delta} T_A \quad (5)$$

For example, if T_C=0, measuring an interval of 1 ns with a resolution of 10ps requires a time of 200 × T_A. If T_A = 4 ns then the measurement time will be approximately 800 ns.

[14] Those skilled in the art will appreciate that time quantizer 30A has a limited valid measurement range. From the waveforms of Figure 4B it can be seen that if: T_d were larger than T_A-DT_B, where D is the duty cycle of clkB, then flip flop 44 will sample a HIGH value on the second rising edge of clkA. This would signal an end of conversion prematurely. It can also be seen that if T_d is less than $|\tau_B - \tau_A|$, where τ_A is the time between the application of the START signal to oscillator 40A and the first rising edge of clkA being applied to flip flop 44 and τ_B is the time between the application of the STOP signal to oscillator 40B and the first rising edge of clkB being applied to flip flop 44 then flip flop 44 will sample a HIGH value on the first rising edge of clkB regardless of the value of T_d. This is because the first rising edge of clkB will occur when clkA is still HIGH.

[15] Range extender block 34 inhibits the operation of coincidence detector 42 until time quantizer circuit 30A is in its valid measurement range. In the illustrated embodiment, a NAND gate 48 is connected between flip flop 44 and counter 46. NAND gate 48 prevents EOC_flag from being applied to preserve the value in counter 46 until range extender block 34 has generated a RE-flag signal.

[16] Range extender block 34 may take various forms. One type of range extender uses a circuit which has delay elements in an input signal path. A range extender 34A

which has this construction is shown in Figure 6A. Another type of range extender uses a circuit which has delay elements in a clock signal path. A range extender 34B which has this construction is shown in Figure 7A.

[17] Range extender circuit 34A comprises four flip flops, two k-bit counters, a k-bit comparator, and two delay elements. Figure 6B is a waveform diagram which illustrates signals at various points in range extender circuit 34A. Counters 70A and 70B respectively count the number of rising edges of clkA and clkB. Both counters are initialized to the same value, preferably zero. Since clkA is started before clkB, after the START signal starts clkA then counter 70A will contain a value M_A which is greater than the value M_B contained in counter 70B. The values of counters 70A and 70B are compared by comparator 72. The output of comparator 72 will go HIGH when $M_A = M_B$. RE_flag is set in response to comparator 72 detecting that $M_A = M_B$.

[18] As noted above, M_A and M_B are initialized to the same value. To prevent RE_flag from being set prematurely, circuit 43A uses a flip flop 73. Flip flop 73 prevents the RE_flag signal from being set until the first rising edge of clkA has occurred, thereby ensuring that counter 70A is ahead of counter 70B.

[19] When $t_{A(j)} - t_{B(i)} < T_A$ then M_B may become equal to M_A for a short period after a rising edge of clkB and before the next rising edge of clkA arrives. This may cause comparator 72 to generate a short pulse 71. Pulses 71 become wider at successive rising edges of clkB. When pulses 71 become sufficiently wide, a pulse 71 can be sampled at the same clkA rising edge by both of flip flops 74A and 74B. When all of flip flops 74A, 74B and 73

are set then the output of AND gate 75 changes state to cause the RE-flag to be set.

[20] Since range extender circuit 34A operates asynchronously, a time diversity sampling technique is used to ensure valid sampling of the output of comparator 72. On each rising edge of clkA, counter 70A registers another count. For a short period after the rising edge of clkA, the output of counter 70A may have a transient random value. This random value, if equal to M_B, may cause comparator 72 to generate a short pulse, or glitch 77A (Fig 6B) at its output. Counter 70B changes its count on the rising edges of clkB. For the same reasons, comparator 72 may generate a glitch 77B at its output shortly after a rising edge of clkB. It is desirable to prevent such glitches from prematurely setting RE_flag.

[21] Delay elements 76A and 76B delay the application of the output of comparator 72 to flip flops 74A and 74B. The signals cmp_out1 and cmp_out2 which are applied to flip flops 74A and 74B respectively are delayed by different amounts τ_2 and $\tau_2 + \tau_1$. Choosing a delay element 76B which causes τ_2 to be longer than the longest expected glitch ensures that neither of flip flops 74A or 74B will be set to HIGH as a result of such glitches.

[22] The glitch width can be expected to be about ½ of the interval $\tau_{CLK\text{-}to\text{-}Q}$, where $\tau_{CLK\text{-}to\text{-}Q}$ is the worst-case CLK-to-Q delay for an output bit of counter 70B. This assumes that the worst case process variation of $\tau_{CLK\text{-}to\text{-}Q}$ is less than about 1/4 $\tau_{CLK\text{-}to\text{-}Q}$. The expected worst case process variation of $\tau_{CLK\text{-}to\text{-}Q}$ may be determined by performing a monte-carlo analysis of the components of counter 70B.

[23] Both of flip flops 74A and 74B must be set before the output of AND gate 75 will change state to set

RE_flag. Delay element 76A causes flip flops 74A and 74B to sample the output of comparator 72 at different times. As the rising edges of clkA and clkB become closer together, the pulses output by comparator 72 become longer in duration. Eventually the pulses are long enough in duration to trigger both of flip flops 74A and 74B on one rising edge of clkA. Delay element 76A is selected to provide a value of τ_1 such that when both of flip flops 74A and 74B are triggered, $t_{B(i)}-t_{A(i)}$ is within the valid range described above. For example, where range extender circuit 34A is made using a 0.35 μm CMOS process then τ_1 may be selected as follows:

$$\tau_1 = T_A - \tau_{clkB\text{-}to\text{-}cmp\_out1} - T_C + 3T_{setup} \quad (6)$$

where $\tau_{clkB\text{-}to\text{-}cmp\_out1}$ is the delay between a rising edge of clkB and a corresponding rising edge of cmp_out1 and T_{setup} is the maximum setup time for flip flop 44.

[24] It is worth noting that range extender block 34 does not affect the ultimate precision or accuracy of any measurements made since it merely ensures that the i^{th} rising edges of clkA and clkB are close enough for measuring by time quantizer 30. Range extender block 34 does not interfere with the path of signals clkA and clkB to EOC_flag. From Figure 6B it can be seen that the range extension provided by range extender circuit 34A is as follows:

$$T_d < (2^k - 1)T_A \quad (7)$$

[25] Figure 7A shows an alternative range extender circuit 34B. Figure 7B shows waveforms at various points in circuit 34B for the example of $T_d = 2.6\ T_A$. The core of circuit 34B comprises k-bit counters 70A and 70B which have outputs connected to a k-bit comparator 72. The

output of comparator 72 is connected to the D inputs of flip flops 78A and 78B. Delay elements 76C and 76D are placed in the clock paths of counter 70A and flip flops 78A and 78B. These delay elements provide signals clkA1 and clkA2 which are delayed versions of clkA. Circuit 34B has the advantage that the desired values for the time delays produced by delay elements 76C and 76D do not depend on other time delays in the circuit. This feature makes range extender circuit 34B especially well adapted for field programmable gate array ("FPGA ") implementations of the invention.

[26] In range extender circuit 34B, counters 70A and 70B are initialized to values which differ by 1. Preferably these counters are initialized to values of 1 and 0 respectively. Counter 70A counts rising edges of clkA2 and counter 70B counts rising edges of clkB. From Figure 7B it can be understood that the number in counter 70A remains larger than the number in counter 70B as long as $t_{A2(i)}-t_{B(i)} > \tau_{A1}+\tau_{A2}$, where τ_{A1} and τ_{A2} are the delays produced by delay elements 76C and 76D respectively. When $t_{A2(i)}-t_{B(i)} < \tau_{A1}+\tau_{A2}$ then M_A becomes equal to M_B for a brief time. This causes comparator 72 to generate a pulse 79. Pulse 79 becomes wider at subsequent rising edges of clkB. When pulse 79 is wide enough that both of flip flops 78A and 78B become set at the same time then RE_flag is set.

[27] Referring now to Figure 5, a dual threshold time quantizer 30B also has two oscillators 40. Oscillators 40A and 40B begin oscillating at the rising edges of START and STOP respectively. In time quantizer 30B, oscillator 40A includes a delay element 50 which selectively provides either a shorter delay or a longer delay depending upon the value of a control signal, CRS_flag. During a first part of a measurement cycle

delay element 50 is set to provide a longer delay. This causes T_Δ to have a relatively large value $T_{\Delta C}$. During a second part of the measurement, control signal CRS_flag controls delay element 50 to provide a smaller delay. This reduces T_Δ to a smaller value $T_{\Delta F}$. Preferably $T_{\Delta C}$ is in the range of 5 times to 30 times greater than $T_{\Delta F}$. Most preferably, $T_{\Delta C}$ is approximately 10 times greater than $T_{\Delta F}$.

[28] During the first part of the measurement cycle the successive rising edges of clkB approach the rising edges of clkA relatively quickly because T_Δ is relatively large. When the rising edges of clkB and clkA are separated in time by a value smaller than a threshold time interval then a coarse/fine resolution control circuit 52 causes control signal CRS_flag to switch delay element 50 to its low delay state. In effect, each measurement begins with a coarse resolution and switches to a fine resolution when the rising edges of clkA and clkB are becoming very close to one another.

[29] In the illustrated embodiment, resolution control circuit 52 comprises a delay line 54 which produces a version of clkA delayed by an interval τ_{fine} at the clock input CLK of a flip flop 56. clkB is connected to the D input of flip flop 56. When rising edges of clkA and clkB are separated by an interval of τ_{fine}, or less, then flip flop 56 changes state and CRS_flag is set. A first counter 58 counts the number (N_{COARSE}) of cycles of clkA which occur during the first part of the measurement cycle. A second counter 59 counts the number (N_{FINE}) of cycles of clkA which occur during the second part of the measurement cycle.

[30] To prevent metastable behaviour of flip flop 56 from causing indeterminate states in counters 58 and 59, resolution control circuit 52 preferably comprises flip

flops 56A and 56B. Flip flops 56, 56A and 56B together comprise a triple flip flop synchronizer as described above.

[31] It can be shown that the numbers counted by coarse counter 58 and fine counter 59 are related to T_d as follows:

$$N_{COARSE}T_{\Delta C} + N_{FINE}T_{\Delta F} = T_d + T_C + T_Q + T_R \qquad (8)$$

where T_d, T_C, T_Q, and T_R, are as described above.

[32] If the error term in Equation (8) is negligible then the time required to take one measurement is given approximately by:

$$T_{meas} = (N_{COARSE} + N_{FINE})T_A = \left(\frac{T_d + T_C - \tau_{fine}}{T_{\Delta C}} + \frac{\tau_{fine}}{T_{\Delta F}} \right) \times T_A \qquad (9)$$

[33] For example, if T_C=0, and τ_{fine}=300ps then measuring an interval of 2ns with $T_{\Delta C}$ =50 ps and $T_{\Delta F}$ =10 ps yields N_{COARSE}=34 and N_{FINE}=30. If T_A = 4 ns then the measurement time will be approximately 256 ns. It can be seen that this is significantly shorter than the time required to take a similar measurement using the single resolution time quantizer 30A.

[34] Preferably resolution control circuit 52 is constructed to allow the value of τ_{fine} to be varied. In the illustrated embodiment, delay line 54 comprises a multiplexer 60 which permits one or more delay elements 61 to be either included or not included in the signal path of delay line 54. When delay elements 61 are included in the signal path of delay line 54, τ_{fine} has a value τ_{fineN} . When delay elements 61 are not included in the signal path of delay line 54, τ_{fine} has a smaller value τ_{fineF}. The ability to vary τ_{fine} permits the noise floor of

time quantizer 30B to be estimated in the manner described below.

[35] The time quantizer circuits described above rely on oscillators 40A and 40B having periods which differ by only a very small amount T_Δ. Any mismatch in the gate delays or interconnect wiring between oscillators 40A and 40B can cause a significant increase in T_Δ. The resolution and accuracy of the time quantizer are degraded if T_Δ increases. The mismatch could also result in $T_B > T_A$. This would prevent the time quantizer from functioning properly.

[36] Oscillators 40 are preferably constructed in a manner which permits T_Δ to be set accurately. This may be done by constructing one or both of oscillators 40 using a plurality of controllable delay elements 41A. Figure 8 shows a pair of oscillators 40 which each include a number of controllable delay elements 41A. Each controllable delay element 41A includes a control line which controls the controllable delay element to provide either a longer delay or a shorter delay. The controllable delay elements 41A are controlled digitally by a resolution adjustment controller 82 to achieve relative values for T_B and T_A such that T_Δ is less than a threshold T_{th}. T_{th} is selected to provide adequate resolution and is preferably user configurable. This threshold may be supplied to the circuit as a 16-bit digital number.

[37] The amount of delay which a controllable delay element can add is given by:

$$\tau_{CDE} = \tau_{CDE(1)} - \tau_{CDE(0)} \qquad (10)$$

where $\tau_{CDE(1)}$ and $\tau_{CDE(0)}$ are the delays provided by the controllable delay element when it is in its longer delay

state and its shorter delay state respectively. Resolution adjustment controller 82 generates control signals for controllable delay elements 41A. At any time the state of controllable delay elements 41A can be represented by a pair of vectors, $\bar{a} = a_0, a_1, \ldots a_n$ and $\bar{b} = b_0, b_1, \ldots b_n$ where each element of the vector represents the state of one of the controllable delay elements 41A. Resolution adjustment controller 82 searches for vectors $\bar{a}$ and $\bar{b}$ which yield an acceptable value for T_d (i.e. $T_d < T_{th}$).

[38] In the currently preferred embodiment of the invention, resolution controller 82 causes time quantizer 30 to measure (in a single resolution mode) two known time intervals T_{ref} and $2\ T_{ref}$. The time intervals may be, for example, the period of accurately known reference signals. The number of counts in counter 46 is obtained for each measurement and the numbers of counts are subtracted from one another to yield a difference N_Δ. Assuming that measurement errors are negligible then N_Δ and T_Δ are related to one another by:

$$T_{ref} = N_\Delta T_\Delta \qquad (11)$$

[39] Since T_{ref} is constant, a larger N_Δ corresponds to a smaller T_Δ. For T_Δ to be smaller than T_{th}, N_Δ must be larger than some corresponding value N_{th}. Resolution adjustment controller switches controllable delay elements 41A between their states until it finds a combination in which $N_\Delta < N_{th}$. The steps implemented by resolution adjustment controller to most efficiently seek appropriate vectors $\bar{a}$ and $\bar{b}$ will depend upon how much delay can be added by each controllable delay element 41A.

[40] Oscillators 40 may be constructed so that all of controllable delay elements 41A are designed to be the same. Process variations will result in variations of the delays provided by the controllable delay elements 41A. Preferably each controllable delay element 41A is constructed so that the nominal delay, T_{step}, added by each controllable delay element is less than ½ T_{th}. This can be done by choosing appropriate sizes for the components used in the controllable delay element 41A.

[41] When this construction is used, as vector ā (or vector b̄) steps through values from 0, …, 0 to 1, …, 1 then T_A can be stepped in increments of ½ T_{th}, or less. As long as the initial difference between T_A and T_B is in the range of $(-½ (n-1)T_{th}, ½(n-1)T_{th})$ then there exist vectors ā and b̄ such that $T_A < T_{th}$.

[42] On a real chip it is difficult to guarantee the uniformity of the steps because the value of T_{step} varies with process variations and is affected by the states of neighbouring controllable delay elements. Assume that $T_{step(l)} < T_{step} < T_{step(u)}$, where $T_{step(l)}$ and $T_{step(u)}$ are the lower and upper 3σ thresholds of the probability density function (PDF) of T_{step} (these thresholds may be estimated by performing monte-carlo simulations of loaded ring oscillators). Then, as long as $T_{step(u)} < T_{th}$, vectors ā and b̄ that satisfy the resolution requirement can generally be found if:

$$-nT_{step(l)} < T_{A0} - T_{B0} < nT_{step(l)} \qquad (12)$$

Where 3σ values of $T_{step(l)}$ and $T_{step(u)}$ are used no more than about 1% of manufactured circuits will fail to be able to meet the desired resolution even though the values of T_{step} are not uniform as a result of process variations. Where 6σ values are used then fewer than about 0.1% of

manufactured circuits will fail to provide the desired resolution.

[43] Resolution adjustment will take the maximum time if all $2n+1$ combinations of vectors $\bar{a}$ and $\bar{b}$ (each combination has a different numbers of 1's in vector $\bar{a}$ or $\bar{b}$) must be tried to achieve the required resolution.

[44] If $T_{step(1)}$ is small relative to T_{th} then larger numbers of controllable delay elements 41A must be provided to ensure that a suitable value for T_δ can be obtained even if $T_{A0} - T_{B0}$ is initially large.

[45] Instead of making the delay provided by all of controllable delay elements 41A the same, oscillators 40 may be designed so that different controllable delay elements 41A provide different delays. Preferably the delays are related to one another in an ascending series to provide resolution adjustment steps of different sizes. Most preferably:

$$\tau_{CDE\,i} = (1 + \xi)\tau_{CDE\,i-1} \qquad (13)$$

where $0 < \xi < 1$ is a constant and τ_{CDEi} is the delay added by an i^{th} one of controllable delay elements of an oscillator 40. For example, an oscillator 40 constructed with a series of controllable delay elements 41A such that $\tau_{CDE1} = 8$ ps and $\xi = 0.5$ can have its period adjusted in steps of 8 ps, 12 ps, 18 ps, 27 ps, 40.5 ps, 60.75 ps and so on.

[46] To guarantee that oscillators 40 can be controlled to provide a value of T_δ smaller than T_{th}, The maximum size of the smallest step (taking into account probable process variations) should be smaller than T_{th}.

[47] Where oscillators 40 are constructed to permit adjustment of T_Δ in steps of different sizes then resolution adjustment controller may take advantage of the fact that both coarser and finer adjustment steps are available. This permits very fine resolutions (for example, resolutions on the order of 5 ps or less) to be achieved while reducing the average adjustment time. A binary search algorithm is preferably used to select vectors $\bar{a}$ and $\bar{b}$ which provide a resolution $T_\Delta < T_{th}$.

[48] In addition to adjusting oscillators 40 to provide a desired value for T_Δ resolution adjustment controller 82 should check to ensure that $T_A > T_B$. A TATB checker circuit 84 may be used to perform this check. Figures 9A and 10A illustrate two alternative TATB checker circuits that may be used in practising this invention. TATB checker circuit 84A of Figure 9A is used by triggering both of oscillators 40A and 40B at the same time (i.e. $T_d = 0$). TATB checker circuit 84A includes a pair of flip flops 85, 86 and a counter 88. As the waveforms of Figure 9B illustrate, when $T_A < T_B$, flip flop 85 samples LOW until the i^{th} rising edge of clkA matches that of clkB. This occurs after $((D\text{-}1)T_A + T_C)/T_\Delta$ cycles of clkA. However, flip flop 86 samples a HIGH value after T_C/T_Δ cycles of clkA. Therefore flip flop 86 is set before flip flop 85.

[49] As seen in Figure 9C, if $T_A < T_B$, the reverse occurs. Resolution adjustment controller 82 can check to ensure that $T_A < T_B$ by monitoring the two flags EOC_flag and ERR1_flag which are set by the outputs of flip flops 85 and 86 respectively. While the condition $T_A < T_B$ is being checked, the reset lines of flip flops 85 and 86 must be inactive. This is ensured in TATB circuit checker 84A by providing an OR gate 89 controlled by resolution

adjustment controller 82. OR gate 89 maintains the reset lines of flip flops 85 and 86 LOW while a check is in progress.

[50] For TATB circuit checker 84A to function properly the integer part of $((D-1)T_A + T_C)/T_\Delta$ must not equal the integer part of T_C/T_Δ . Otherwise, both flags may be set in the same cycle of clkA. This requirement will generally be satisfied by typical designs. For example, in a circuit implementation in a 0.35 µm CMOS process, $(D-1)T_A$ is 1.5 ns, maximum T_C is 0.4 ns and maximum T_Δ is 0.15 ns. In the worst case the integer part of $((D-1)T_A + T_C)/T_\Delta$ is 12 while the integer part of T_C/T_Δ is 2.

[51] Since setup and hold times for flip flops 85 and 86 could be different, flip flops 85 and 86 might be set high simultaneously on the first or second rising edges of clkA and clkB. Such a case results in decision deadlock. The alternative TATB checker circuit 84B of Figure 10A addresses this problem but is more complicated than circuit 84A. Circuit 84A may share components with time quantizer 30. for example, flip flop 85 may be the same flip flop as flip flop 44 of Figure 4.

[52] It can be seen from the waveforms of Figure 10B that counter 70A (Fig. 6A) will count faster than counter 70B as long as $T_A < T_B$. This causes $M_A - M_B$ to increase as time passes. Assuming that T_d=0 the initial difference between the values in counters 70A and 70B will be either 0 or 1. If this difference becomes 2 or more then it must be the case that $T_A < T_B$. TATB circuit checker 84B has a pair of counters 90A and 90B. Comparator 92 compares the values in counters 90A and 90B. Counter 90B is initialized to a value which is 2 larger than the initial

value of counter 90A. For example, counters 90B and 90A are initialized to values of 2 and 0 respectively.

[53] If the values in counters 90A and 90B become equal then comparator 92 generates a signal at its output which indicates that $T_A < T_B$. The techniques for reliably detecting when the values in counters 90A and 90B are equal which are described above in respect of range extender circuits 34A or 34B are preferably also used in TATB circuit checker 84B. In the embodiment illustrated in Figure 10A the delayed clock signals clkA1 and clkA2 from range extender circuit 34B are connected to the clock inputs of flip flops 93 and 94.

[54] TATB circuit checker 84B may share components with other circuits which are not required to operate while a TATB check is being performed. For example, counter 90A may comprise at least 3 significant bits of counter 70A of Figure 4.

[55] If controllable delay elements 41A all provide substantially the same variation in T_d then one method that can be implemented in resolution adjustment controller 82 for selecting vectors $\bar{a}$ and $\bar{b}$ is to perform an exhaustive search. Resolution adjustment controller may comprise a $2n$-bit state machine where n is the number of controllable delay elements 41A in each of oscillators 40A and 40B. n of the state machine's output bits are connected to the n controllable delay elements of oscillator 40A and the other n output bits are connected to the n controllable delay elements of oscillator 40B. The state machine cycles through all possible combinations of a distinct vector $\bar{a}$ with a distinct vector $\bar{b}$ (in this case, two versions of a vector $\bar{a}$ are not considered distinct unless they have the different number of 1's. For example, $\bar{a}$=1100000 is not considered

distinct from ā=1000100 because both of these vectors have two 1's in them). Figure 11A shows steps in one possible exhaustive search method 100A for selecting vectors ā and b̄. If all distinct combinations of vectors ā and b̄ have been tried and no combination which provides an acceptable T_Δ has been found then an error signal is generated.

[56] One disadvantage of performing an exhaustive search is that it can be unnecessarily time consuming. To reduce time, an alternative method, 100B, which is shown in Figure 11B may be used. Method 100B checks only distinct vectors ā if $T_A < T_B$ and checks only distinct vectors b̄ if $T_A > T_B$. This reduces the number of combinations that must be checked.

[57] Where oscillators 40 are constructed with controllable delay elements which are designed to add different delays when activated then the exhaustive search strategy becomes less practical because it requires a much larger number of combinations of vectors ā and b̄ to be checked. Up to 2^{2n} combinations may need to be checked in the worst case. An exhaustive search can be implemented easily by providing a 2*n*-bit counter in resolution adjustment controller 82 as shown in Figure 12.

[58] A semi-exhaustive search can be performed with the similar hardware. The semi-exhaustive search increments either ā or b̄, depending upon whether $T_A > T_B$ or $T_B > T_A$. Figure 13 is a flow chart which illustrates steps in a semi-exhaustive search method. In a semi-exhaustive search the maximum number of combinations tested is 2^n.

[59] Figure 14 depicts steps in a fast search method 110 that may be implemented in resolution adjustment

controller 82. In method 110 if $T_A<T_B$ only ā is adjusted because T_A must be adjusted to obtain an acceptable value for T_A. Similarly, if $T_A>T_B$, only b̄ is adjusted to increase T_B. Since oscillators 40A and 40B are made to be very similar to one another, T_A and T_B will likely be initially close to one another. Therefore, the first choice is ā =0..0 and b̄=0..0. If $N_A < N_{th}$, the lowest significant bit of ā (or b̄) (depending on whether $T_A<T_B$ or $T_A>T_B$) is set high to increase T_A (or T_B) by the smallest amount possible. If the required resolution is still not achieved, the next bit of ā or b̄ is set HIGH and all other bits are set LOW. This is continued until setting the i-th bit HIGH implies that or T_A (or T_B) has been increased too much. Then the i-th and (i-1)-th bits are set LOW and HIGH, respectively, and the process starts over by setting the 0-th bit. To illustrate method 110, assume that $T_A>T_B$, n=6 and the required resolution is ultimately achieved for b̄ =001001. The algorithm goes through the following sequence to find the required b̄: 000000, 000001, 000010, 000100, 001000, 010000, 001001. This is in contrast with the exhaustive and semi-exhaustive searches, which go through the following sequence: 000000, 000001, 000010, 000011, 000100, 000101, 000110, 000111, 001000, 001001. As can be seen from above, the fast algorithm finds the solution in 7 steps, while the exhaustive and semi-exhaustive search each require 10 steps.

[60] Controllable delay elements 41A can take any of various forms. Some types of controllable delay element may be made with standard digital cells. A controllable delay element may comprise a logic gate having a capacitive load provided by a load element. The load element permits the capacitive load to be digitally switched to different values. Each load element comprises

a digital switch and a load. Turning on the switch increases the load applied to output of the corresponding logic gate. This results in a longer propagation delay. Figures 15A through 15E illustrate various types of load elements and their simplified models.

[61] In designing load elements it is preferable to minimize the cell area required to provide a time difference T_{diff}. It is also desirable that T_{diff} should be relatively insensitive to variations in the control voltage V_{ctrl}. If T_{diff} varies with fluctuations in V_{ctrl} then any noise in V_{ctrl} will add jitter to oscillators 40. This will increase T_R with the result that time quantizer 30 will have reduced precision.

[62] In the following description, $C_{gs(X)}$, $C_{gd(X)}$, $C_{gb(X)}$, $C_{db(X)}$, and $C_{sb(X)}$ are respectively the gate-source, gate-drain, gate-bulk, drain-bulk and source-bulk capacitances of the transistor M_X, where X is a transistor identifier. Values for $S^{T_{diff}}_{V_{ctrl}}$ are listed in Table I for various types of load element.

[63] Figure 15A shows a voltage-controlled NMOS load element 112A. Although element 112A provides a relatively large T_{diff} in a small area, T_{diff} is quite sensitive to V_{ctrl} because the equivalent capacitive loading of cell is a function of V_{ctrl}.

[64] Figure 15B shows a load element 112B in which the capacitive load is a capacitance 113. A simple model for such a load element has an ideal switch S, the switch resistance R_S, the switch drain capacitance $C_{d(S)} = C_{db(S)} + C_{gd(S)}$, the switch source capacitance $C_{s(S)} = C_{sb(S)} + C_{gs(S)}$, and the load capacitance C_L. R_S is in the range of a few tens of MΩ when switch 114 is OFF and a few KΩ when switch 114

is ON. As is evident in the model, the $C_{d(S)}$ and $C_{s(S)}$ are also loading the oscillator. Since $C_{db(S)}$, $C_{gd(S)}$, $C_{sb(S)}$, and $C_{gs(S)}$ are functions of V_{ctrl}, this style of load element has a high T_{diff} sensitivity to V_{ctrl} and is therefore not preferred. Any load element having a switch connected to the oscillator node suffers from this high sensitivity characteristic.

[65] Figure 15C shows an alternative load element 112C and its simple model. In the model, $C_{d(S)} = C_{db(S)} + C_{gd(S)}$. This design provides a low T_{diff} sensitivity to V_{ctrl} because when switch transistor M_S is ON, the impedance of $C_{d(S)}$, $Z_{d(S)} = \frac{1}{2\pi f C_{d(S)}} >> R_S$. Therefore, the $C_{d(S)}$ variations do not affect the total loading provided by load element 112C significantly. Note also that variation in R_S due to V_{ctrl} does not affect the capacitive loading of the cell significantly. If the M_S area is large such that $C_L << C_{d(S)}$ and $Z_{d(S)}$ dominates (i.e. $Z_{d(S)} << R_S$), then the load variation due to V_{ctrl} variations is not significant because: $C_{L(eon)} = C_L C_{d(S)} / (C_L + C_{d(S)}) - C_L$. In this case, the effect of R_S is significantly diminished, which means that the load variations for ON and OFF states of switch M_S are small. This is a disadvantage when larger load variations are required. Therefore, special attention must be paid to switch size in this design. Load element 112C has the advantage that it occupies a small area for a given load. However, fabricating a load element 112C requires that the target technology permit fabrication of floating capacitors.

[66] Figure 15D shows a load element 112D similar to load element 112C except that a NMOS gate capacitor is used instead of a parallel-plate capacitor. In the associated model, $C_{g(L)} = C_{gs(L)} + C_{gd(L)}$ and $C_d = C_{sb(L)} + C_{db(L)} + C_{db(S)} + C_{dg(S)}$. The sensitivity of T_{diff} to variations in V_{ctrl}

is only marginally greater than that of load element 112C. In the prototype implementation, described below a load element 112D is used because it provides 10 ps delay in an area of a single-drive NOT gate and it exhibits low sensitivity to variations in V_{ctrl}.

[67] The load element 112E of Figure 15E shows a good insensitivity to variations in V_{ctrl} but requires more area to achieve a given delay than does load element 112D. In the model for load element 112E, $C_{d(L)} = C_{gs(L)} + C_{gd(L)}$ and $C_d = C_{gb(L)} + C_{db(S)} + C_{dg(S)}$.

[68] Table I shows values for T_{diff} for the load elements of Figures 15A through 15E. The numbers in Table I are for a test configuration shown in Figure 16 in which either 1, 2, 3, 4, 5, or 6 load elements were turned on. Table II shows values for the sensitivity of T_{diff} to variations in V_{ctrl}.

TABLE I. T_{diff} for various control voltages

V_{ctrl}	2.5V	2.6V	2.7V	2.8V	2.9V	3V	3.1V	3.2V	3.3V
a1	24.3	25.9	27.4	28.9	30.2	31.5	32.8	34	35.2
a2	75.7	80.3	84.7	89	93.4	97.7	101.6	105.8	109.5
a3	154.6	162.9	170.9	179.8	187.9	195.9	203.7	211.2	218.7
a4	269.1	284	299.1	314.2	328.5	342.7	356.2	369.4	382.1
a5	423.8	447.5	471.5	495	518.2	540.4	561.1	581.8	601.8
a6	636.4	672.7	708.7	743.5	777.7	811.1	843.4	875.1	905.2
b1	57.4	61.6	65.89	70.2	74.3	78.4	82.4	86.5	90.2
b2	142.8	153.2	163.6	173.9	184.3	194.7	204.7	214.6	224.3
b3	250.2	268.8	287.3	306.1	324.6	342.9	361	378.9	396.4
b4	387.5	417.3	446.9	476.5	506.4	535.6	564.8	593.8	622.2
b5	555	598.3	642.3	686.2	730.1	773.9	817.1	859.9	902.5
b6	771.5	834.7	898.6	962.8	1020	1090	1150	1210	1280
c1	34.8	34.8	34.9	34.9	34.9	35	35	35	35
c2	121.1	121.3	121.4	121.5	121.6	121.7	121.9	121.9	122.1
c3	262.4	262.8	263.1	263.4	263.8	264	264.2	264.3	264.6
c4	484	484.9	485.7	486.4	486.9	487.5	488	488.4	488.9
c5	789.4	791	792.4	793.5	794.5	795.4	796.3	797	797.84
c6	1248	1251	1253	1255	1257	1259	1260	1262	1263
d1	9.44	9.47	9.43	9.44	9.45	9.39	9.44	9.55	9.49
d2	33.19	33.25	33.35	33.53	33.59	33.67	33.69	33.73	33.8
d3	73.19	73.4	73.62	73.95	74.19	74.33	74.37	74.59	74.62
d4	130.3	131.1	131.5	131.9	132.3	132.8	133.1	133.4	133.7
d5	210.6	211.7	212.5	213.2	213.9	214.6	215.2	215.7	216.3
d6	316.9	318.7	320.6	321.6	323	324	325.1	326.2	327.1
e1	0.844	0.825	0.904	0.757	0.891	0.938	0.952	0.791	0.761
e2	3.33	3.27	3.3	3.26	3.35	3.16	3.47	3.19	3.31
e3	7.14	7.16	7.18	7.28	7.42	7.14	7.27	7.15	7.31
e4	15.72	15.83	15.68	15.73	15.71	15.73	15.75	15.82	15.77
e5	28.17	28.42	28.25	28.49	28.29	28.41	28.41	28.41	28.62
e6	49.38	49.47	49.56	49.4	49.46	49.47	49.56	49.53	49.48

Table II

	$\frac{\Delta T_{diff}}{\Delta V_{ctrl}}$	$S^{T_{diff}}_{V_{ctrl}}$		$\frac{\Delta T_{diff}}{\Delta V_{ctrl}}$	$S^{T_{diff}}_{V_{ctrl}}$		$\frac{\Delta T_{diff}}{\Delta V_{ctrl}}$	$S^{T_{diff}}_{V_{ctrl}}$
a1	13.5	1.3	b1	40.9	1.5	c1	0.308	0.03
a2	42.2	1.3	b2	101.9	1.5	c2	1.23	0.03
a3	80.2	1.2	b3	182.8	1.5	c3	2.77	0.03

a4	141.2	1.2	b4	293.4	1.6	c4	6.09	0.04
a5	222.6	1.2	b5	434.4	1.3	c5	10.55	0.04
a6	336	1.2	b6	636.7	1.64	c6	18.35	0.408
d1	0.06	0.02	e1	-0.1	-0.45			
d2	0.755	0.07	e2	-0.3	-0.3			
d3	1.78	0.08	e3	0.211	0.1			
d4	4.23	0.104	e4	0.594	0.124			
d5	7.1	0.108	e5	0.569	0.07			
d6	12.72	0.128	e6	0.123	0			

[69] Controllable delay elements 41A may also be based on standard digital cells. This is preferable because there are some situations where it is not possible or practical to update a digital library for fabricating an oscillator for use in the invention. Figures 17A and 17B show two controllable delay elements 115A and 115B which each use a multiplexer 116 to select between two path segments for insertion into a signal path. Such controllable delay elements are useful especially where the controllable delay element should exhibit a large delay difference between its long delay and short delay states. Process variations typically cause different multiplexers made according to the same design to exhibit significant differences in propagation delays. These process dependent variations could mask small differences in delay between the two path segments. A multiplexer-based controllable delay element is particularly useful for achieving a delay increment step of about 40 ps or more.

[70] The delay difference in the two multiplexed path segments can be achieved by providing a different number of delay elements in the two path segments, as shown in figure 17A or by loading a delay element in one path

segment differently from a corresponding gate element in the other multiplexed path segment as shown in figure 17B. The construction shown in Figure 17B is preferred where 20 ps < τ_{CDE} < 60 ps. The construction shown in Figure 17A is preferred where τ_{CDE} > 60 ps.

[71] For achieving a very small τ_{CDE} on the order of a few picoseconds, one of the controllable delay elements of Figure 18A, 18B or 18C may be used. In controllable delay element 117A of Figure 18A, a logic gate 119 is loaded by the input of a tri-state NOT-gate (tri-NOT) 120. The delay of the element increases when tri-NOT 120 is activated.

[72] Figures 19A and 19B show two typical tri-NOT gate implementation as can be found in standard cell libraries. When the tri-NOT gate of Figure 19A is inactive, the load C_{gdp} + C_{gdn} is floating because these capacitances are in series with large impedances (transistors M1 and M4 are in high impedance mode). When M1 and M4 are turned on, these capacitances are added to the capacitive load on the input of the tri-NOT. A similar effect occurs when a tri-NOT as shown in Figure 19B is activated. A value of τ_{CDE} of 3 ps or less may be obtained in a controllable delay element 117A made with standard 0.35 µm CMOS fabrication processes.

[73] The additional capacitative loading provided by a tri-NOT gate when it is activated is a small percentage (typically about 5% to 10%) of its total loading. A controllable delay element 117A therefore is particularly useful where a very small value of τ_{CDE} is required. As shown in Figures 18B and 18C the value of τ_{CDE} can be changed by either using a different tri-state buffer as a

load element or by adding additional load elements at the output of gate 119.

[74] Figure 20 shows a controllable delay element 122 which comprises a number of similar logic gates and tri-state gates connected in parallel. All of the gates should provide similar functions and have similar propagation delays. If they do not then logic contentions may occur at the outputs of each element. In the illustrated embodiment, a NOT gate 123 is connected in parallel with a tri-NOT gate 124. When it is inactive, the tri-NOT gate 124 contributes only an output load. NOT gate 123 provides drive current as well as load. When tri-NOT gate 124 is activated, it adds a small load to the output load and some drive current to the total drive. Depending on which of the additional load or drive current has the dominating effect the delay will increase or decrease. The delay which can be controlled by a controllable delay element 122 can be estimated by:

$$\tau_{CDE} = V_{dd}\left[\frac{C_\Delta/I_\Delta - C_{o(0)}/I_{o(0)}}{1 + I_{o(0)}/I_\Delta}\right] \qquad (14)$$

where $C_{o(0)}$ and $I_{o(0)}$ are the output capacitance and drive current of delay element 122 when tri-NOT 124 is inactive and C_Δ and I_Δ are the additional capacitance and drive current when tri-NOT 124 is active.

[75] Delay element 122 has the disadvantage that it suffers from large process variations. However, it may be used with good results for mid range values of τ_{CDE} (in the range of, for example, 20 ps to 50 ps). Delay element 122 has the advantage that it can be implemented with devices from a digital library which includes tri-state buffers but does not include tri-NOT gates. A delay

element 122 can, for example, be implemented on a FPGA. In many FPGA block cells the only available tri-state devices are tri-state buffers.

[76] A TDC 22 according to the invention is calibrated before it is used. Where time quantizer 30 is a single resolution quantizer (for example in a time quantizer which uses circuit 30A), the relationship between N and T_d is linear. Therefore, if one knows T_C and T_Δ then it is straightforward to calculate T_d from N. To estimate T_C and T_Δ two accurately know time intervals T_{cal1} and T_{cal2}, which may be supplied from off-chip, are measured. The resulting numbers N_1 and N_2 are recorded. It can be seen that:

$$N_{cal1}T_\Delta = T_{cal1} + T_C + T_{Q1} + T_{R1} \qquad (15)$$

and,

$$N_{cal2}T_\Delta = T_{cal2} + T_C + T_{Q2} + T_{R2} \qquad (16)$$

where T_{Q1} and T_{Q2} are quantization errors, and T_{R1} and T_{R2} are random errors associated with the first and second measurements respectively. Preferably T_{cal1} and T_{cal2} are chosen so that $N_{cal1}-N_{cal2} > 200$.

[77] T_C and T_Δ may be estimated using a two-point calibration, in which case T_{C0}, the estimated value of T_C is given by:

$$T_{C0} = \frac{T_{cal2}N_{cal1} - T_{cal1}N_{cal2}}{N_{cal2} - N_{cal1}} \qquad (17)$$

and $T_{\Delta 0}$, the estimated value of T_Δ is given by:

$$T_{C0} = \frac{T_{cal2} - T_{cal1}}{N_{cal2} - N_{cal1}} \qquad (18)$$

[78] It can be shown that the error associated with the estimation of T_Δ is a random variable having a mean of zero and a variance given by:

$$\sigma^2_{T_{\Delta e}} = \frac{T_\Delta^2}{6(N_{cal2} - N_{cal1})^2} + \frac{2\sigma_R^2}{(N_{cal2} - N_{cal1})^2} \qquad (19)$$

The error associated with the estimation of T_C is also a random variable having a mean of $-T_\Delta/2$ and a variance given by:

$$\sigma^2_{T_{Ce}} = \left(\frac{T_\Delta^2}{12} + \sigma_R^2 \right) \times \frac{(1 + N_{cal2}/N_{cal1})^2}{(1 - N_{cal2}/N_{cal1})^2} \qquad (20)$$

[79] A more accurate estimate of T_C and T_Δ may be estimated using an n-point calibration. For an n-point calibration, n accurately known time intervals are measured by TDC 22. These time intervals are multiples of a reference interval. An objective of n-point calibration is to limit the range of T_Q variations and to therefore reduce σ_{Tce}.

[80] Since a low-jitter reference clock is often available on a chip for two-point or n-point calibration, it is convenient to choose $T_{cal1} = T_{ref}$, $T_{cal2} = 2T_{ref}$, ... , $T_{caln} = nT_{ref}$. A circuit 130 that allows reliable generation of KT_{ref} intervals is shown in Figure 21A. In circuit 130, when Cal=0, the Ref signal is connected to the clk inputs of flip flops 132 and 133. Since the D input of flip flop 133 is always HIGH, START is set high at the first rising edge of the Ref signal. The STOP signal always is set HIGH one Ref cycle after SP_In turns HIGH. Since the K_DGen state machine block 134 sets SP_In to HIGH (K-1) cycles after the rising edge of the Ref signal, A delay of K Ref cycles results between the edges of START and

STOP. The waveforms in Fig 21B illustrate the operation of circuit 130 for K=0, 1 and 2.

[81] Constant delay is generated in the path of calibration signals in this circuit. The same delay will be used in the actual measurement, except for the term $\Delta\tau_{MUX1} - \Delta\tau_{MUX2}$ which represents the variation of the difference in propagation delays from I0 and I1 inputs to output in the multiplexers MUX1 and MUX2, respectively. This is important for making absolute measurements because, if the mismatch is significant, the value estimated for T_c during calibration will not be the same as the one used in actual measurements. This would cause additional error.

[82] Therefore, the Ref signal paths to clk inputs of flip flops 132 and 133 must be matched to the IN1 and IN2 signal paths to the same inputs, respectively. This is particularly important in high resolution measurement because on-chip matching of elements to a high resolution is very difficult. Here, it is assumed that this matching is achieved, and therefore the term $\Delta\tau_{MUX1} - \Delta\tau_{MUX2}$ is negligible. This matching is not required when the calibration is being performed for making differential measurements because T_c does not affect the accuracy or precision of differential measurements.

[83] Where a double resolution time quantizer 30 is used (for example, where the time quantizer circuit 30B of Figure 5 is used) each measurement generates two numbers. To estimate $T_{\Delta(C)}$ and $T_{\Delta(F)}$ system 20 may perform a number M_{cal} of measurements of known time intervals. In a preferred embodiment of the invention, the i^{th} measurement set includes the following three measurements:

1. $T_{d(i,1)} = T_{ref}$ and, $\tau_{fine} = \tau_{fine1}$. Therefore:

$$N_{c(i,1)}T_{\Delta(c)} + N_{f(i,1)}T_{\Delta(f)} = T_{d(i,1)} + T_C + T_{Q(i,1)} + T_{R(i,1)} \quad (21)$$

2. $T_{d(i,2)} = 2T_{ref}$ and $\tau_{fine}=\tau_{fine1}$. Therefore:

$$N_{c(i,2)}T_{\Delta(c)} + N_{f(i,2)}T_{\Delta(f)} = T_{d(i,2)} + T_C + T_{Q(i,2)} + T_{R(i,2)} \quad (22)$$

3. $T_{d(i,3)} = 4T_{ref}$ and $\tau_{fine}=\tau_{fine2}$. Therefore:

$$N_{c(i,3)}T_{\Delta(c)} + N_{f(i,3)}T_{\Delta(f)} = T_{d(i,3)} + T_C + T_{Q(i,3)} + T_{R(i,3)} \quad (23)$$

[84] Each of these measurements is made M times and the resulting three sets of M equations are averaged over i=1, …, M_{cal} to yield the following equations:

$$\overline{N_{c(i,1)}}T_{\Delta(c)} + \overline{N_{f(i,1)}}T_{\Delta(f)} = \overline{T_{d(i,1)}} + T_C + \overline{T_{Q(i,1)}} + \overline{T_{R(i,1)}} \quad (25)$$

$$\overline{N_{c(i,2)}}T_{\Delta(c)} + \overline{N_{f(i,2)}}T_{\Delta(f)} = \overline{T_{d(i,2)}} + T_C + \overline{T_{Q(i,2)}} + \overline{T_{R(i,2)}} \quad (26)$$

$$\overline{N_{c(i,3)}}T_{\Delta(c)} + \overline{N_{f(i,3)}}T_{\Delta(f)} = \overline{T_{d(i,3)}} + T_C + \overline{T_{Q(i,3)}} + \overline{T_{R(i,3)}} \quad (27)$$

[85] For sufficiently large values of M_{cal}, $T_{R(j)}$ and $T_{Q(j)}$ average to negligible values. Choosing $T_{d(i,1)}=T_{ref}$, $T_{d(i,2)}=2T_{ref}$, and $T_{d(i,3)}=4T_{ref}$ is desirable because it simplifies circuit design. Assuming that noise factors are negligible, subtracting equation (26) from (25) and equation (27) from (26) yields the following system of equations:

$$N_{c(21)}T_{\Delta(c)} + N_{f(21)}T_{\Delta(f)} = T_{ref} \quad (29)$$

and,

$$N_{c(31)}T_{\Delta(c)} + N_{f(31)}T_{\Delta(f)} = 3T_{ref} \quad (30)$$

where:

$$\begin{aligned} N_{c(21)} &= \overline{N_{c(2)}} - \overline{N_{c(1)}} & N_{f(21)} &= \overline{N_{f(2)}} - \overline{N_{f(1)}} \\ N_{c(31)} &= \overline{N_{f(3)}} - \overline{N_{f(1)}} & N_{f(31)} &= \overline{N_{f(3)}} - \overline{N_{f(1)}} \end{aligned} \quad (31)$$

[86] Solving this system of equations provides accurate estimates for T_Δ and T_c. It is important to note that $T_{d(i,3)}$ is measured while $\tau_{fine}=\tau_{fine2}$ because this assures

that the determinant of equations (29) and (30) is large enough to preserve the estimation accuracy.

[87] System 22 can be used to make various types of measurement. One jitter characteristic that can be measured is RMS jitter. RMS jitter can be defined as follows:

$$J_{RMS} = \sqrt{\frac{1}{M}\sum_{i=1}^{M}(T_{d(i)} - \overline{T}_d)^2} \qquad (32)$$

where M is the number of samples taken and $T_{d(i)}$ is the time interval measured for the i-th jitter sample.

[88] Estimating J_{RMS} is often sufficient for jitter testing. It can be shown that an estimate of J_{RMS} is given by:

$$J_{RMS}^2 = T_{RMS}^2 + \frac{T_\Delta^2}{12} + \sigma_R^2 \qquad (33)$$

where σ^2_R is the total RMS internal jitter of TDC 30. T_Δ is known through calibration. If TDC 30 is well characterized then σ^2_R will also be known. Therefore, an accurate estimate of RMS jitter can be obtained.

[89] The error in this estimate can be shown to be inversely proportional to M. Therefore, this error can be made to be very small by using a large value for M. M may be, for example, in excess of 500 and is preferably in the range of 1000 to 2500. In designing a TDC 30 for use in estimating RMS jitter it is more important to minimize σ^2_R than it is to minimize T_Δ because the value of T_Δ can be determined accurately during calibration of TDC 30.

[90] The variance in internal jitter of time quantizer 30 increases with the number of cycles it takes to complete a measurement. The internal jitter in time quantizer 30 can be estimated by performing two sets of measurements after calibration using a double resolution time quantizer. A first set of measurements is taken with $\tau_{fine}=\tau_{fine1}$. The result is a set of pairs of counts N_{c1}, and N_{f1}. The second set of measurements is taken with $\tau_{fine}=\tau_{fine2}$. The result is a set of pairs of counts N_{c2}, and N_{f2}. The second set of counts has the same single shot accuracy as the first set of counts. However, each measurement in the second set takes more cycles of clkA to complete because $\tau_{fine2}<\tau_{fine1}$. In the second set of measurements, a larger proportion of each measurement is carried out in the fine resolution mode.

[91] Since the second set of measurements take longer to complete, the total measured RMS jitter in the second set of measurements is greater than the RMS jitter in the first set of measurements. Since the input signal is the same, the internal jitter of time quantizer 30 can be determined. If we assume that the internal jitter of time quantizer 30 appears as white noise then the internal jitter in the second set of measurements will scale with a factor α relative to the internal jitter in the second set of measurements with α given by:

$$\alpha = \frac{\overline{N_2}}{\overline{N_1}} \qquad (34)$$

where $N_1=N_{c1}+N_{f1}$ and $N_2=N_{c2}+N_{f2}$. If the noise is Gaussian it is possible to achieve measurement accuracy of 0.1 ps using this technique by choosing a large M. For example, RMS jitter in a 10 MHz signal could be measured with 0.1 ps accuracy by taking approximately M=300,000 samples.

[92] For testing jitter tolerance and jitter transfer characteristics of devices such as clock recovery units ("CRUs") it is necessary to supply the CRU with a signal that has a known jitter. Figure 22 shows a circuit 140 which may be used to generate a signal having known jitter characteristics. A jitter-free clock signal is supplied to circuit 140. Circuit 140 includes a delay line 141, a multiplexer 142 and a sequence counter 143. The multiplexer connects a selected tap of delay line 141 to output J in response to a control signal from sequence counter 143. Sequence counter 143 specifies which tap is connected to output J at any clock edge. For example, if delay line 141 has 8 taps and sequence counter 143 is a three bit up/down counter then circuit 140 will generate a triangular shaped jitter signal with a maximum peak-to-peak amplitude of 7_g where 7_g is the delay introduced by each delay element of delay line 141. By using a counter with a sequence which follows a sinusoidal pattern, circuit 140 will generate a signal having jitter which varies sinusoidally with time. Sequence counter 143 may be programmable so that circuit 140 can generate various types of jitter signal at its output J.

[93] A TDC 22 may be used on-chip to measure period jitter. A histogram approach can provide statistics of such jitter. TDC 22 can measure period jitter by causing edge sampler 24 to make a number of measurements. In each measurement the edge sample passes two consecutive rising (or falling) edges of a signal V_{in} being measured to time quantizer 30 as START and STOP signals. After this has been done, control circuit 26 reads the value(s) of N stored in the counter(s) of time quantizer 30, passes these values to an analysis system and commences another measurement. This can be repeated until a desired number of samples has been taken. Figure 23 shows an edge

sampler circuit that may be used in making period jitter measurements.

[94] The analysis system will typically be an external tester but may also be on chip. Where the analysis system is external then the data collected is transmitted to the analysis system through a suitable interface. For example, the chip may comprise a serial bus such as a JTAG interface or a parallel interface for moving the data off-chip. Preferably an on-chip data storage area is provided to hold the collected data while it is waiting to be delivered to the analysis system.

[95] The analysis system can form a histogram of the data and calculate variance and peak-to-peak jitter. If the analysis system receives information about the time at which each sample was taken then it can also analyze frequency components of the jitter. Thus, appropriately configured systems according to the invention may be used to conduct full jitter compliance tests.

[96] In some applications, such as serial communications it is necessary to measure jitter between corresponding edges of two different signals. For example, without loss of generality corresponding edges of two signals might be required to fall within a tight time window. Figure 24A shows an edge sampler circuit 150 that can be used to generate START and STOP signals for measuring jitter between two signals IN1 and IN2. In circuit 150, flip flop 151 samples an edge of IN1 and flip flop 152 samples an edge of IN2 which is closes to the sampled edge of IN1. A delay element 153 ensures that the output of flip flop 151 has enough time to be set before the edge of IN2 arrives. This will be the case if:

$$t_{IN2} > t_{IN1} - \tau_{D2} + \tau_{q1} + \tau_{s2} \qquad (35)$$

where τ_{q1} is the CLK-to-Q delay of flip flop 151, τ_{s2} is the setup time of flip flop 152, and τ_{D2} is the delay introduced by delay element 153.

[97] Figure 24B is a timing diagram which shows waveforms at various points in edge sampler circuit 150 for one positive and one negative value of $T_J = t_{IN1} - t_{IN2}$. The generated START and STOP signals are passed to TDC 22 for measurement of the time displacement between them. After a measurement is completed, flip flops 151 and 152 are reset and another measurement can be taken. While the sample and hold times of flip flops 151 and 152 affect the measured time displacements, these times are constant and affect all measurements equally. They can therefore be dealt with by calibration. Further, it is typically the fluctuation in measured values between measurements that is of interest. These fluctuations are not affected by constant offsets.

[98] Relative jitter tests can be used to perform jitter tolerance limit tests of CRUs. This can be done by applying a signal with a known jitter to the CRU and then measuring the relative jitter between this input signal and a signal output from the CRU.

[99] For production tests of CRUs it is desirable to test jitter tolerance at at least two frequencies, one frequency within the loop bandwidth of the CRU and another frequency outside the loop bandwidth of the CRU.

Example

[100] A TDC according to the invention has been implemented in 0.35 µm /CMOS technology. In one embodiment the circuit occupies an area equivalent to 1200 2-input NAND gates and provides a time resolution of

approximately 4 ps (~1/5 of a gate delay in current standard 0.35 µm CMOS technology). The TDC generates a digital signature which can be read out by an inexpensive tester for further analysis to obtain the jitter characteristics of the signal being measured.

[101] Figure 25 is a top level diagram of a TDC made according to the invention. In this example embodiment of the invention uniform controllable load elements have been designed as standard cells to allow for automatic place and route. The rest of the cells used in the implementation have been taken from a standard digital cell library.

[102] The jitter measurement system of Figure 25 has the following blocks:

- TQ: Time Quantizer;
- RE-TATB: Range extender and TA > TB condition checker;
- Main Counter and DivBy2 circuit;
- REEOC-sync-DFF, TQEOC-sync-DFF and ERRI-sync-DFF: RE-EOC, TQ-EOC and ERRI-flag synchronizer flip-flops;
- TATB Check Delay Gen: Generates a small time delay for checking TA > TB; and,
- Delay Generator: Controls the selection of the delays needed for resolution adjustments, calibration and measurement.

[103] Six different controllable load elements have been designed according to the style of Figure 15D. The transistor sizes for each of these cells are given in Table III. The forth row of table III lists the additional delay in the oscillator A or B obtained by activating the cell. These controllable load elements

allow for ±288ps or ±8.5% period mismatch between clkA and clkB (this is obtained when all the controllable load elements are activated). The last row of Table III lists the area of each cell. The height of all the cells is the standard cell library height. The area of the smallest cell is equivalent to the area of a double-drive 2-input NAND gate.

TABLE III - Example Controllable Load Elements

	CL_0	CL_1	CL_2	CL_3	CL_4	CL_5
M_S [w µm / l µm]	4 0.35	4 0.35	4 0.35	4 0.35	4 0.35	4 0.35
M_L [w µm / l µm]	3 0.5	6 0.5	9 0.5	13.5 0.5	18 0.5	27 0.5
Delay (ps)	11	23	35	50	67	101
Area (w(µm x h µm)	6.3x21	7.9x21	9.4x21	9.4x21	11x21	14x21

[104] Oscillators 40A and 40B in the TQ block each have a signal path which loops through 11 NAND gates and one AND gate. Six taps for each oscillator are connected to six different controllable load elements. The outputs of oscillators 40A and 40B are directly connected to the clk and D inputs of flip flop DFF_EOC. These outputs are buffered before being used in other control blocks which are less time sensitive. The output of flip flop DFF-EOC is sampled and held by another flip-flop to ensure that the end-of-conversion signal, EOC-Flag, can be observed by the control blocks operating with the system clock.

[105] In addition to START and STOP inputs, two other inputs have been reserved for applying StartCheck and StopCheck signals to oscillators A and B, respectively (see Figure 26). These inputs are used to apply a T_d for the purpose of checking the condition $T_A > T_B$. Without these inputs, an additional multiplexer would be required. However, when START and STOP are applied to the

time quantizer the StartCheck and StopCheck signals must he inactive (HIGH), and vice versa. The main controller block ensures this condition using four control signals, Main-Set, rbMain, CheckSet, and rbCheck. The flip-flop TQEOC-sync-DFF is provided to synchronize the TQ-EOC signal with the system clock, SCLK, in order to avoid sampling errors by the Main-Controller block.

[106] The implementation of the RE-TATB block is essentially as described above with k = 6, τ_{A1}= 1.2 ns and τ_{A2} = 0.4 ns. The flip-flop REEOC-sync-DFF synchronizes the RE-EOC signal with the system clock, SCLK. This prevents errors in sampling by the Main Controller block. Buffers Buf1 to Buf6 are not necessary and are included to perform mixed signal simulations. Figure 27 is a schematic diagram for RE-TATB while Figures 27 and 28 show the 3-bit and 6-bit comparators used in RE-TATB.

[107] A 16-bit synchronous counter is used to count the number N. As shown in Fig. 4, clkA could drive the counter's clock input directly. However, the maximum operational frequency of the 16-bit counter used in this example is 250 MHz, whereas clkA has a frequency of 350 MHz. A divide by 2 divider circuit DivBy2 divides clkA by two. Thus enables the counter to count the number of clkA edges. The state of the DivBy2 circuit recovers the lost bit due to division as follows:

$$N = 2N_{cntr16} - clkDiv2 \qquad (36)$$

where N_{cntr16} is the state of the 16-bit counter and clkDiv2 is the state of the DivBy2 flip flop. If the frequency of clkA is so high that even the frequency of clkDiv2 is too high for the counter a 2-bit or 3-bit ripple counter could be used in place of one divider to divide the clkA frequency by 4 or 8. The overflow bit of such counter can be used as the clock for the main counter.

[108] The delay generator block generates START and STOP edges with $t_{stop} - t_{start} = T_{ref}$, $2T_{ref}$ and $(t_{IN2}-t_{IN1})$ for [SelD1, SelD0]=[01], [10], and [11] respectively. When [SelD1, SeID0]=[00], both START and STOP are set HIGH and the StartCheck and StopCheck signals are activated to check for the condition $T_A > T_B$. This block is illustrated in Figure 30.

[109] TATB Check Delay Generator generates a delay of 1.8 nsec between the StartCheck and StopCheck edges in the $T_A > T_B$ check mode. The outputs of this block are set HIGH in other modes. A schematic of this block is shown in Figure 31.

[110] The main controller monitors the outputs of all other blocks and generates required signals for controlling the operation of the TDC. The main controller may be specified using synthesizable Very High Speed Integrated Circuit Hardware Description Language ("VHDL") code. The TDC operation starts by loading a threshold N_{th} serially. The serial data is read through SThre input while TestStart is HIGH. Then, the controller controls the Delay Generator while the TATB Check Delay Generator block performs resolution adjustment. After adjustment, calibration is performed and the TDC switches to measurement mode.

[111] The Main Controller controls the "TATB Check Delay Generator" and "Delay Generator" to generate appropriate signals for three different time quantization modes, 'TA > TB check', 'Nth evaluation', and 'sample measurement'. The first two modes are used in resolution adjustment and calibration while the last mode is used after calibration to measure jitter samples.

[112] The timing diagram of Figure 31 shows the behaviour of some important signals during these three modes. During all three modes, first MainSet, rbMain, CheckSet, and rbCheck are all set LOW for five cycles of the system clock (SCLK) to ensure both oscillators 40A and 40B are in their reset states. Consequently, in '$T_A > T_B$ check' mode, rbMain and MainSet are set HIGH while rbCheck and CheckSet are set LOW. This causes START and STOP signals to be set HIGH. The time quantizer is then ready to accept StartCheck and StopCheck signals.

[113] At the next SCLK edge, rbCheck turns HIGH and two SCLK cycles after that, StartCheck and StopCheck signals are generated. When '$T_A > T_B$ check' is completed, MainSet, rbMain, CheckSet, and rbCheck are all set LOW again.

[114] In 'N_{ch} evaluation' and 'sample measurement' modes, after the five reset SCLK cycles, rbCheck and CheckSet are set HIGH while rbMain and MainSet are set LOW. This causes StartCheck and StopCheck signals to be set HIGH. The time quantizer is then ready to accept START and STOP signals. At the next SCLK edge, rbMain turns HIGH and on the following SCLK edge, START and STOP signals are generated. When time quantizer operation is completed, MainSet, rbMain, CheckSet, and rbCheck are all set LOW again.

[115] In measurement mode, the Main Controller instructs the Delay Generator block to pass jitter samples to the time quantizer. Upon completion of each measurement, the data is sent off-chip serially through the DataOut output. The InputReady, MeasReady, and DataReady signals are used for handshaking between the external tester and TDC.

[116] In the foregoing disclosure, conventional elements, such as power supply connections and the like are not

specifically discussed or illustrated in the drawings. Such elements are well known to those skilled in the art and have been omitted for clarity.

[117] Those skilled in the art will appreciate that the circuits and methods described herein have various advantages. Among these are that the invention may be practised with circuits which are entirely digital and are well adapted to being designed using conventional design tools including automatic place and route. Jitter measurements having an accuracy in the order of 10ps can be attained. The digital and compact nature of this TDC circuit makes it very attractive for BIST applications for testing high-speed serial communication interfaces, e.g., clock and data recovery, timing circuits, and edge placement circuits. Since the TDC provides a very high-resolution time measurement capability, it is also suitable for use in testing digital clock recovery and clock synthesis circuits. It is also notable that oscillators 40A and 40B integrate power supply noise (which is non-random). High frequency power supply noise is effectively cancelled. If oscillators 40A and 40B are made structurally very similar to one another they will be affected in substantially the same manner by any low frequency power supply noise. Therefore, low frequency power supply noise can be effectively cancelled as well.

[118] As will be apparent to those skilled in the art in the light of the foregoing disclosure, many alterations and modifications are possible in the practice of this invention without departing from the spirit or scope thereof. For example, it will be understood from the foregoing that in systems according to various embodiments of the invention:

- time delay elements may be inserted in places where their effects can be compensated for in hardware or software;
- logic levels may be reversed and hardware modifications made to preserve the function of the circuits in question.

[119] Accordingly, the scope of the invention is to be construed in accordance with the substance defined by the following claims.

WHAT IS CLAIMED IS:

1. A time to digital converter comprising:

a timing circuit (30) comprising first and second digital oscillators (40A, 40B) producing first and second clock signals (clkA, clkB) respectively, the first and second oscillators having different periods (T_A, T_B);

at least one of the oscillators comprising a plurality of digitally controllable delay elements (41A), the delay elements, when activated altering the period of the oscillator;

a coincidence detector connected to generate a coincidence signal (EOC_flag)when a reference point in the first clock signal has a known time relationship to a corresponding reference point on the second clock signal;

a first counter connected to count a number (N) of cycles of the first oscillator until the coincidence detector generates the coincidence signal; and,

a resolution adjustment circuit connected to start the first and second oscillators at times separated by a known interval (T_{ref}), compare the number N to a threshold (N_{th}) and, if N is not at least equal to a threshold value altering the period of at least one of the oscillators by activating or deactivating one or more of the digitally controllable delay elements (41A).

2. The time to digital converter of claim 1 wherein the first and second oscillators are switchable between a first state wherein a difference in periods of the first and second signals is $T_{\Delta 1}$ and a second state wherein a difference in periods of the first and second signals is $T_{\Delta 2}$ where $T_{\Delta 2} < T_{\Delta 1}$; and,

the time to digital converter comprises:

a resolution switching control circuit connected to switch the timing circuit from its first state to its second state;

a second counter connected to count a number (N_c) of edges of the first signal between a START signal and a time when the timing circuit is switched from its first state to its second state, the first counter connected to count a number (N_p) of edges of the first signal between the time when the timing circuit is switched from its first state to its second state and the time when coincidence signal is generated.

3. The time to digital converter of claim 2 wherein the resolution switching control circuit comprises a delay element connected to provide a delayed first clock signal and a coincidence detector (56) connected to generate a coincidence signal (CRS_flag) when a reference point in the second clock signal has a known time relationship to a corresponding reference point on the delayed first clock signal.

4. The time to digital converter of claim 3 wherein the delay element is selectively configurable to provide one of at least two different delays.

5. The time to digital converter of claim 3 wherein the delay element comprises a multiplexer (60) connected to a plurality of signal path segments, at least one of the second signal path segments comprising at least one gate (61A, 61B), the delayed first clock signal passing through one of the signal path segments selected by the multiplexer.

6. The time to digital converter of any one of claims 1 through 5 comprising a range extender circuit, the range extender circuit suppressing the coincidence signal (EOC_flag) until corresponding edges of the first and second clock signals are within one cycle of one another.

7. The time to digital converter of claim 6 wherein the range extender circuit comprises a first k-bit counter (70A) connected to count edges of the first signal (clkA), a second k-bit counter (70B) connected to count edges of the second signal (clkB) and a comparator (72) connected to compare outputs of the first and second k-bit counters and the resolution switching control circuit generates a resolution switching signal (RE_flag) when a pulse at the comparator output exceeds a predetermined length.

8. The time to digital converter of claim 7 wherein the predetermined length is determined by a delay element (76B) coupled between an output (cmp_out) of the comparator and a flip flop (74B).

9. The time to digital converter of claim 7 wherein the predetermined length is determined by a delay element (76D) coupled between the first clock signal (clkA) and an input to the first k-bit counter (70A).

10. The time to digital converter of any one of claims 1 through 9 wherein the first and second oscillators comprise ring oscillators each comprising a closed signal path defined at least in part by a plurality

of series connected delay elements each having an input and an output.

11. The time to digital converter of claim 10 wherein the controllable delay elements each comprise a gate having an input and output connected in the signal path and a variable load element connected to the output.

12. The time to digital converter of claim 11 wherein the variable load element comprises a tri-state device having an input connected to the output of the gate.

13. The time to digital converter of claim 12 wherein the tri-state device comprises a tri-NOT gate.

14. The time to digital converter of claim 10 wherein the load element comprises an NMOS gate capacitor connected in series between the output of the gate and a digital switch.

15. The time to digital converter of claim 10 wherein a gate electrode of the NMOS gate capacitor is connected to the output of the gate.

16. The time to digital converter of any one of claims 1 through 15 wherein each of the oscillators comprises a plurality of digitally controllable delay elements.

17. The time to digital converter of claim 16 wherein all of the plurality of digitally controllable delay elements provide substantially the same effect on the period of the oscillator when activated.

18. The time to digital converter of claim 16 wherein, each of the oscillators the plurality of digitally controllable delay elements comprises a series digitally controllable delay elements which provide delays τ_{CDE} related to one another by $\tau_{CDE(i)} = (1+\xi)\tau_{CDE(i-1)}$.

19. A time to digital converter comprising:

a timing circuit comprising first and second digital oscillators producing first and second clock signals respectively, the first and second oscillators switchable between a first state wherein a difference in periods of the first and second signals is $T_{\Delta 1}$ and a second state wherein a difference in periods of the first and second signals is $T_{\Delta 2}$ where $T_{\Delta 2} < T_{\Delta 1}$;

a resolution switching control circuit connected to switch the timing circuit from its first state to its second state when the reference point of the first clock signal approaches the known time relationship with the reference point of the second clock signal;

a coincidence detector connected to generate a coincidence signal (EOC_flag) when a reference point in the first clock signal has a known time relationship to a corresponding reference point on the second clock signal;

a first counter connected to count a number (N_F) of edges of the first clock signal between the time when the timing circuit is switched from its first state to its second state and the time when the coincidence signal is generated; and, a second counter connected to count a number (N_C) of edges of the first signal between a START signal and a time when the timing circuit is switched from its first state to its second state.

20. The time to digital converter of claim 19 wherein the resolution switching control circuit comprises

a delay element connected to provide a delayed first clock signal and a coincidence detector (56) connected to generate a coincidence signal (CRS_flag) when a reference point in the second clock signal has a known time relationship to a corresponding reference point on the delayed first clock signal.

21. The TDC of claim 20 wherein the delay element has a first state resulting in a first delay of the delayed first clock signal and a second state resulting in a second delay of the delayed first clock signal different from the first delay.

22. A digital timing circuit for generating first and second digital output signals having first and second periods, the timing circuit comprising:

a first ring oscillator triggered by a first control signal (START) and generating a first clock signal (clkA);

a second ring oscillator triggered by a second control signal (STOP) and generating a second control signal (clkB);

at least one of the oscillators comprising a plurality of digitally controllable delay elements (41A), the delay elements, when activated altering the period of the oscillator;

a coincidence detector connected to generate a coincidence signal (EOC_flag) when a reference point in the first clock signal has a known time relationship to a corresponding reference point on the second clock signal;

a counter connected to count a number (N) of cycles of the first oscillator between the first control signal and the coincidence signal; and,

a resolution adjustment circuit connected to generate the first and second control signals at times separated by a known interval (T_{ref}), compare the number N to a threshold (N_{th}) and, if N is not at least equal to a threshold value altering the period of at least one of the oscillators by activating or deactivating one or more of the digitally controllable delay elements (41A).

23. A method for producing first and second digital signals having first and second periods, the method comprising:

a) providing a pair of digital oscillators;

b) starting the first oscillator and starting the second oscillator a time period T_d after starting the first oscillator;

c) counting a number N of cycles of the first oscillator until a reference point on the first signal coincides with a corresponding reference point on the second signal;

d) if N is not at least equal to a threshold value altering the period of at least one of the oscillators and repeating steps (b) and (c) until N is at least equal to the threshold value.

24. The method of claim 23 wherein varying a period of at least one of the oscillators comprises changing a state of a controllable delay element.

25. The method of claim 23 comprising, if N exceeds a second threshold, altering the period of at least one of the oscillators and repeating steps (b) and (c) until obtaining an N between the first and second thresholds.

26. A method for time to digital conversion comprising providing first and second digital oscillators having periods which differ by an amount T_Δ wherein the first and second oscillators are switchable between a first state wherein a difference in periods of the first and second signals is $T_{\Delta 1}$ and a second state wherein a difference in periods of the first and second signals is $T_{\Delta 2}$ where $T_{\Delta 2} < T_{\Delta 1}$;

starting the first oscillator upon the occurrence of a first control signal and starting the second oscillator on the occurrence of a second control signal a time T_d later;

when the reference points occur within a known time delay of one another switching the oscillators to their second state;

counting a number (N_C) of edges of the first clock signal which occur between the first control signal and a time when the oscillators are switched to their second state; and,

counting a number (N_F) of edges of the first clock signal which occur between the time when the oscillators are switched to their second state and a time when the reference points have a known time relationship.

27. The method of claim 26 wherein the reference points are edges of the first and second signals and the known time relationship is coincidence of the edges.

28. The method of claim 26 comprising estimating a noise floor for the first and second oscillators by acquiring a first set of the numbers N_F and N_C for T_d having a known value T_{ref} while the known time delay has a first value and a second set of the numbers N_F and N_C for T_d having a known value T_{ref}, or a known

multiple of T_{ref}, while the known time delay has a second value, averaging N_F and N_C for each set of measurements and computing the noise floor from the average values of N_F and N_C for the two sets of measurements.

29. A frequency tunable digital ring oscillator comprising a closed signal path defined at least in part by a plurality of series connected delay elements each having an input and an output the delay elements comprising at least one digitally controllable delay element, the digitally controllable delay element comprising a gate connected in series with the signal path and a tri-state device having an input connected to an output of the gate and a control connection connected to a control device.

30. The digital ring oscillator of claim 29 wherein the tri-state device comprises a tri-NOT gate.

31. The digital ring oscillator of claim 29 wherein the tri-state device comprises a tri-state buffer.

32. The digital ring oscillator of any one of claims 29 through 31 comprising *n* digitally controllable delay elements each having a tap and the oscillator comprises an *n*-bit state machine having one output connected to each of the taps.

33. Any apparatus or method described herein whether or not claimed in any of claims 1 through 32.

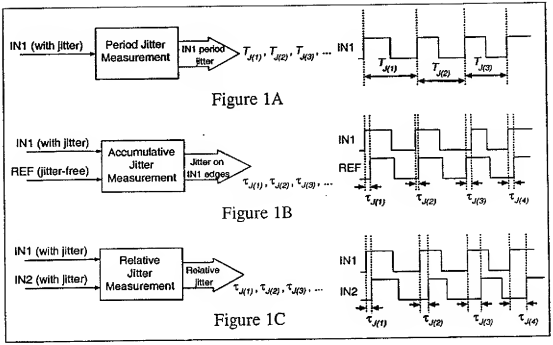


Figure 1A

Figure 1B

Figure 1C

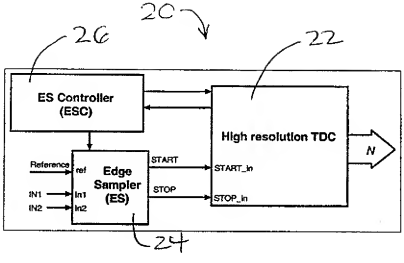

20
26
22
ES Controller
(ESC)
High resolution TDC
N
Reference
ref
Edge
Sampler
(ES)
START
STOP
START_in
STOP_in
IN1
In1
IN2
In2
24

Figure 2

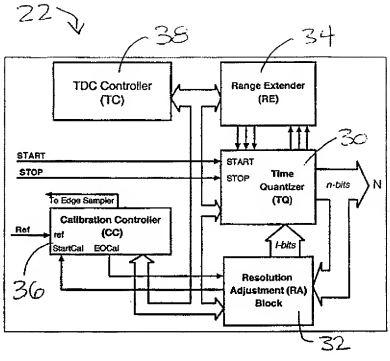

22
38
34
TDC Controller
(TC)
Range Extender
(RE)
30
START
STOP
START
STOP
Time
Quantizer
(TQ)
n-bits
N
To Edge Sampler
Calibration Controller
(CC)
Ref
ref
StartCal
EOCal
I-bits
36
Resolution
Adjustment (RA)
Block
32

Figure 3

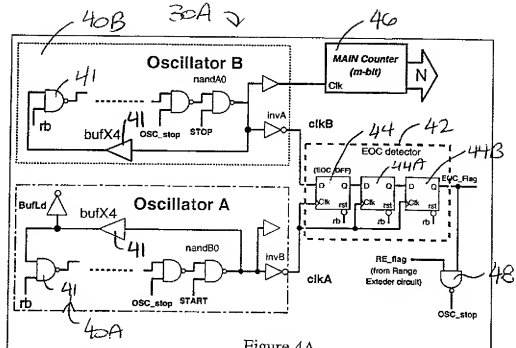


Figure 4A

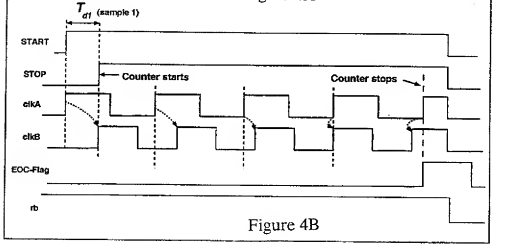


Figure 4B

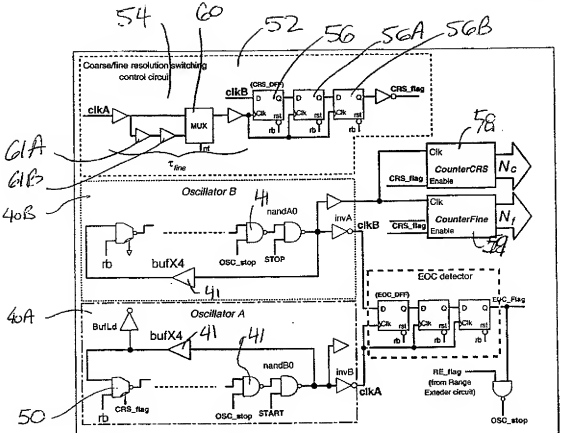


Figure 5A

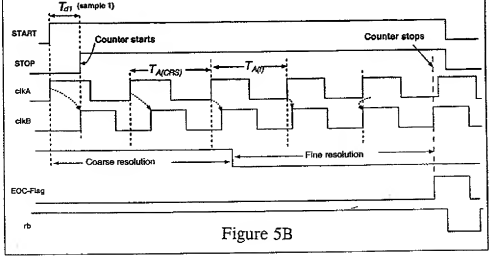


Figure 5B

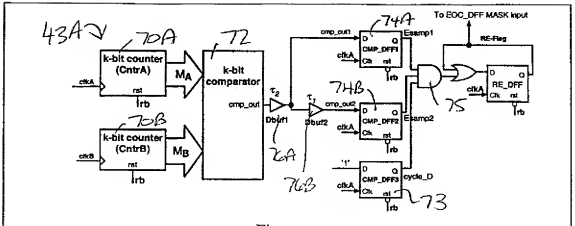


Figure 6A

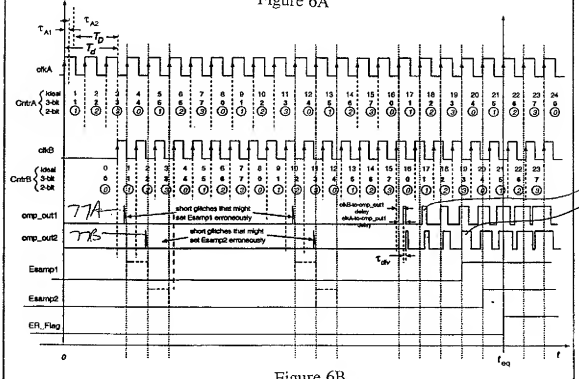


Figure 6B

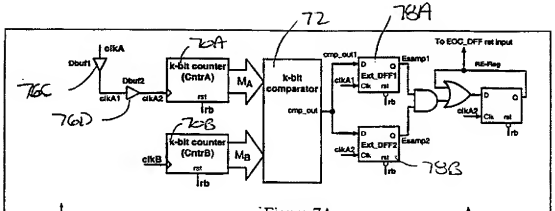


Figure 7A

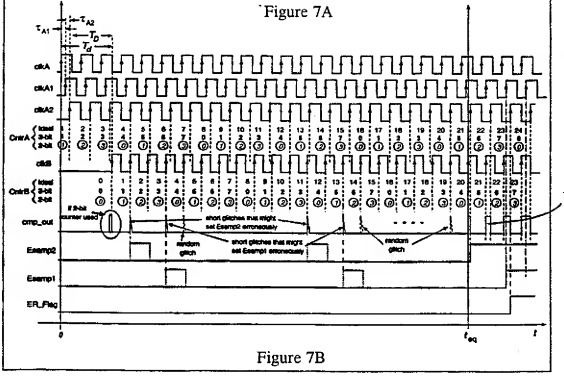


Figure 7B

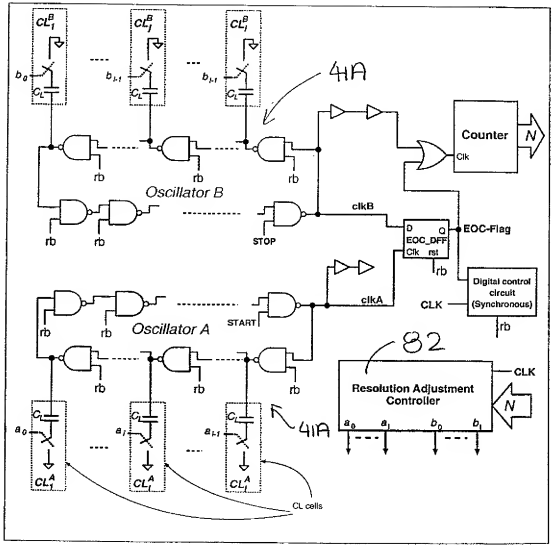

4IA
Counter
N
Clk
Oscillator B
rb
clkB
STOP
D
Q
EOC_DFF
Clk
rst
EOC-Flag
Digital control circuit (Synchronous)
CLK
clkA
START
Oscillator A
82
Resolution Adjustment Controller
CL cells

Figure 8

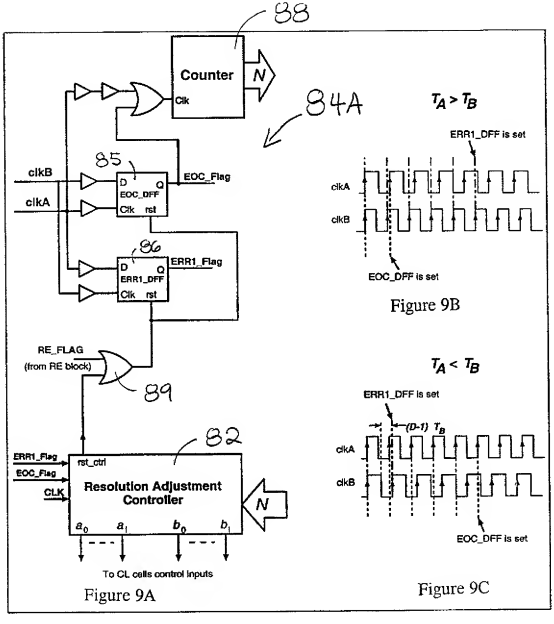
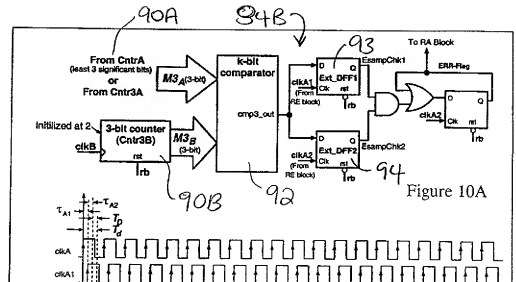


Figure 9A

Figure 9B

Figure 9C


90A
94B
93
To RA Block
From CntrA
(least 3 significant bits)
or
From Cntr3A
M3A(3-bit)
k-bit
comparator
ESampChk1
ERR-Flag
Ext_DFF1
clkA1
(From
RE block)
Clk
nrt
rb
D
Q
Initilized at 2
3-bit counter
(Cntr3B)
clkB
M3B
(3-bit)
cmp3_out
clkA2
Ext_DFF2
ESampChk2
94
90B
92
Figure 10A

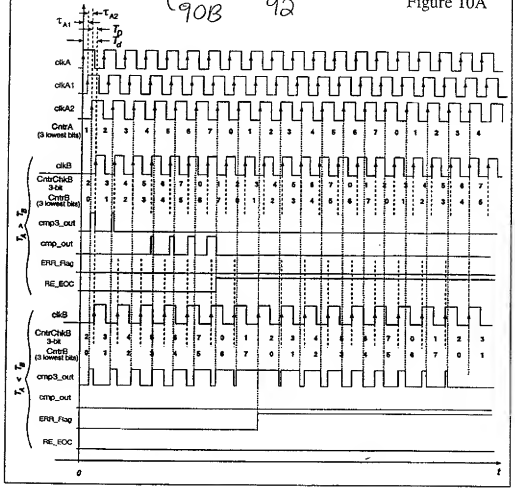

clkA
clkA1
clkA2
CntrA
(3 lowest bits)
clkB
CntrChkB
3-bit
CntrB
(3 lowest bits)
cmp3_out
cmp_out
ERR_Flag
RE_EOC
0
t

Figure 10B

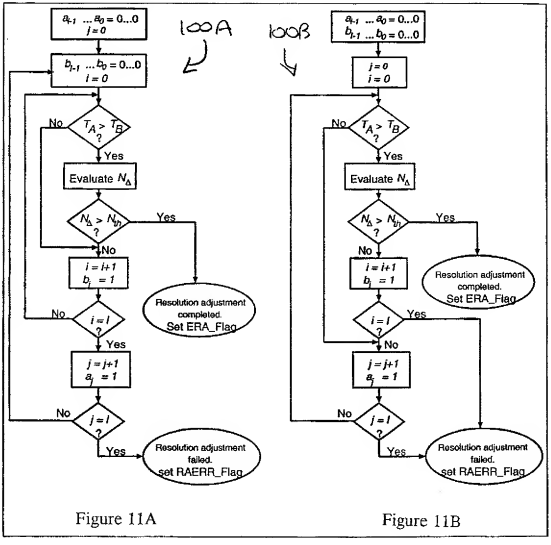


Figure 11A

Figure 11B

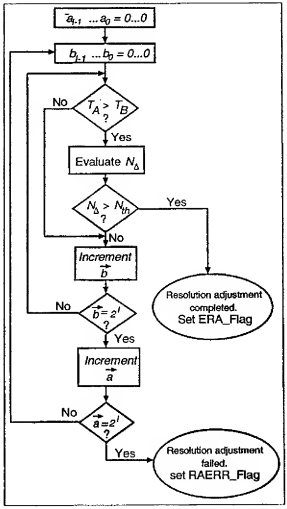

$\vec{a}_{i-1} \ldots a_0 = 0 \ldots 0$
$\vec{b}_{i-1} \ldots b_0 = 0 \ldots 0$
No
$T_A > T_B$?
Yes
Evaluate N_Δ
$N_\Delta > N_{th}$?
Yes
No
Increment $\vec{b}$
Resolution adjustment completed. Set ERA_Flag
No
$\vec{b} = 2^i$?
Yes
Increment $\vec{a}$
No
$\vec{a} = 2^i$?
Yes
Resolution adjustment failed. set RAERR_Flag

Figure 12

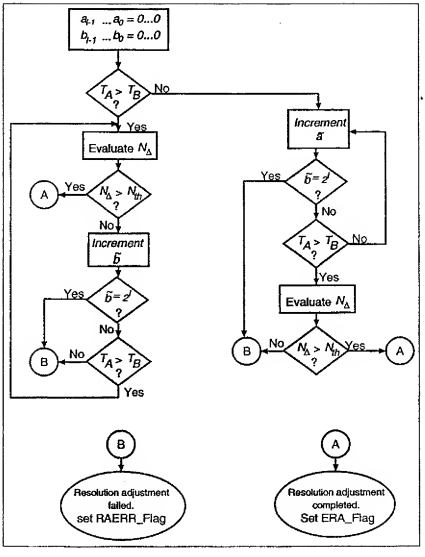

$a_{i-1} \ldots a_0 = 0 \ldots 0$
$b_{i-1} \ldots b_0 = 0 \ldots 0$
$T_A > T_B$?
No
Yes
Evaluate N_Δ
A
Yes
$N_\Delta > N_{th}$?
No
Increment $\vec{b}$
Yes
$\vec{b} = \vec{2}$?
No
B
No
$T_A > T_B$?
Yes
Increment $\vec{a}$
Yes
$\vec{b} = \vec{2}$?
No
$T_A > T_B$?
No
Yes
Evaluate N_Δ
B
No
$N_\Delta > N_{th}$?
Yes
A
B
Resolution adjustment failed.
set RAERR_Flag
A
Resolution adjustment completed.
Set ERA_Flag

Figure 13

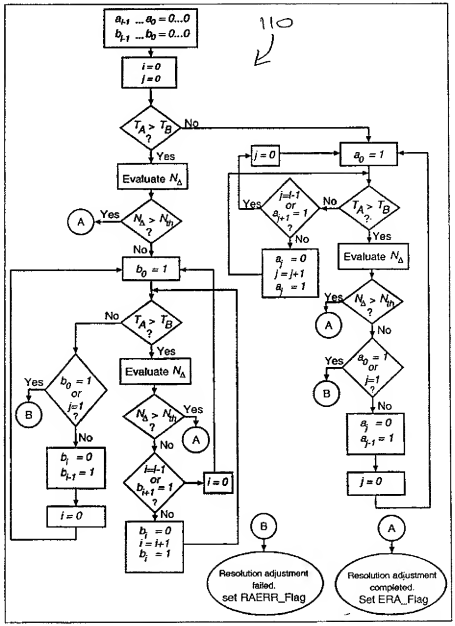
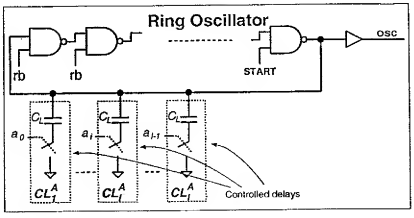

110
$a_{i-1} \ldots a_0 = 0 \ldots 0$
$b_{j-1} \ldots b_0 = 0 \ldots 0$
$i = 0$
$j = 0$
$T_A > T_B$?
No
Yes
Evaluate N_Δ
$N_\Delta > N_{th}$?
Yes
A
No
$b_0 = 1$
$T_A > T_B$?
No
Yes
Evaluate N_Δ
$N_\Delta > N_{th}$?
Yes
A
No
$i = i+1$ or $b_{i+1} = 1$?
$i = 0$
No
$b_i = 0$
$i = i+1$
$b_i = 1$
$b_0 = 1$ or $j = 1$?
Yes
B
No
$b_i = 0$
$b_{i-1} = 1$
$i = 0$
$j = 0$
$a_0 = 1$
Yes
$j = i-1$ or $a_{j+1} = 1$?
No
$a_j = 0$
$j = j+1$
$a_j = 1$
$T_A > T_B$?
Yes
Evaluate N_Δ
$N_\Delta > N_{th}$?
Yes
A
No
$a_0 = 1$ or $j = 1$?
Yes
B
No
$a_j = 0$
$a_{j-1} = 1$
$j = 0$
B
Resolution adjustment failed.
set RAERR_Flag
A
Resolution adjustment completed.
Set ERA_Flag

Figure 14

Figure 16



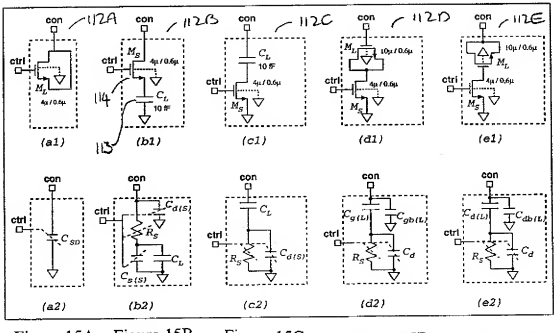


Figure 15A Figure 15B Figure 15C Figure 15D Figure 15E

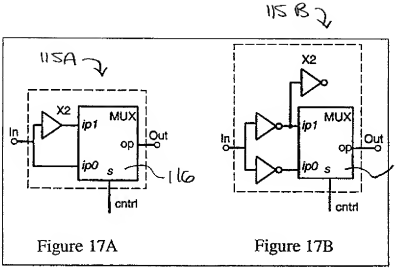


Figure 17A Figure 17B

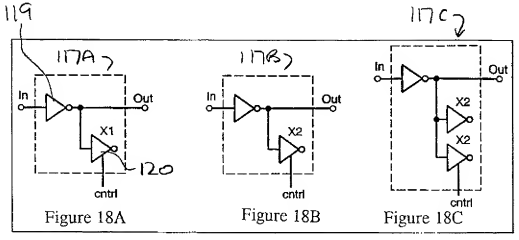


Figure 18A Figure 18B Figure 18C

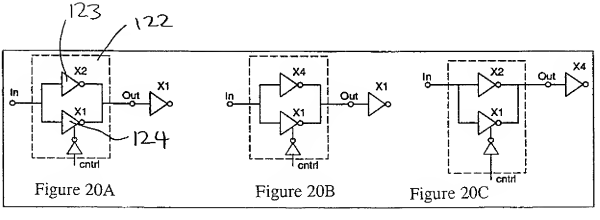


Figure 20A Figure 20B Figure 20C

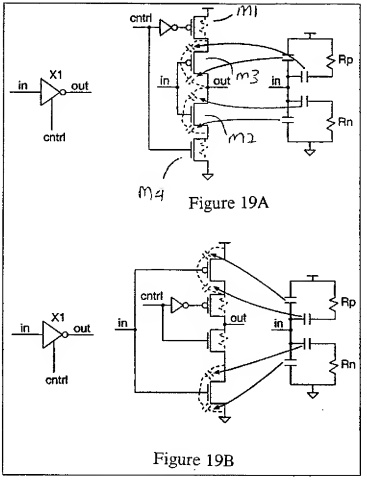


Figure 19A

Figure 19B

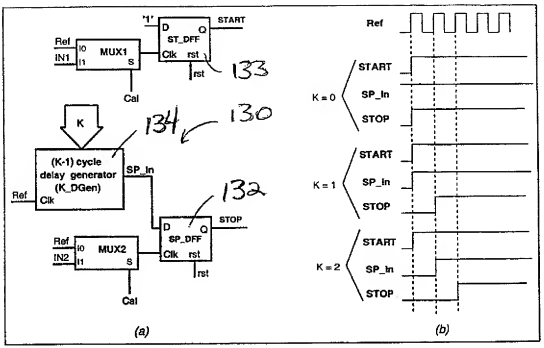

'1'
D
Q
START
ST_DFF
Clk
rst
rst
Ref
I0
IN1
I1
MUX1
S
Cal
133
K
134
130
(K-1) cycle
delay generator
(K_DGen)
Ref
Clk
SP_In
132
STOP
SP_DFF
IN2
MUX2
(a)
Ref
START
SP_In
STOP
K = 0
K = 1
K = 2
(b)

Figure 21

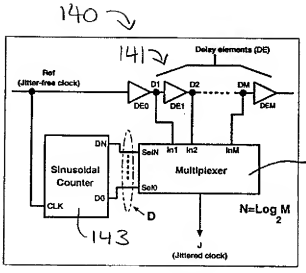


Figure 22

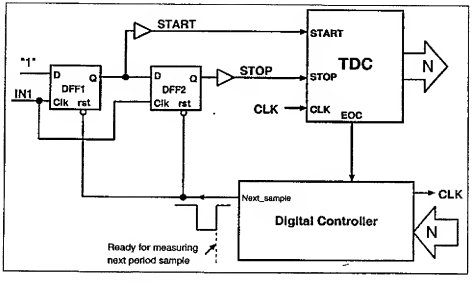


Figure 23

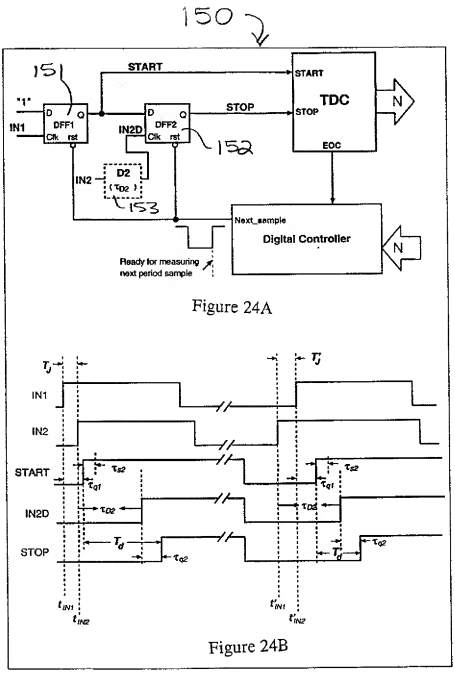


Figure 24A

Figure 24B

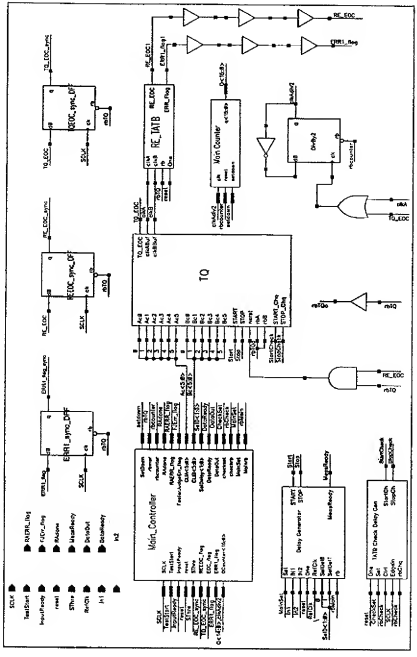


Figure 25

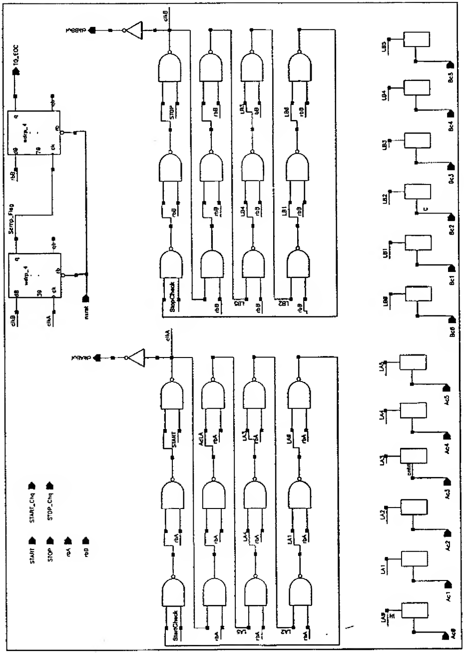


Figure 26

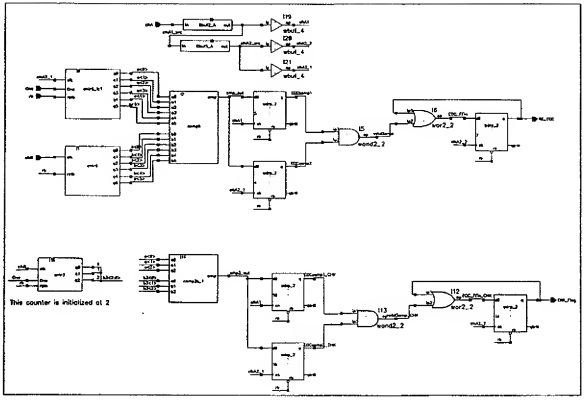


Figure 27

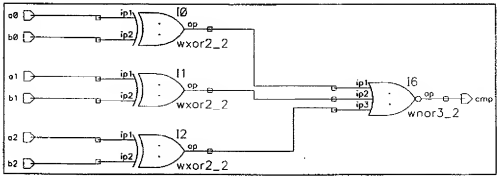


Figure 28

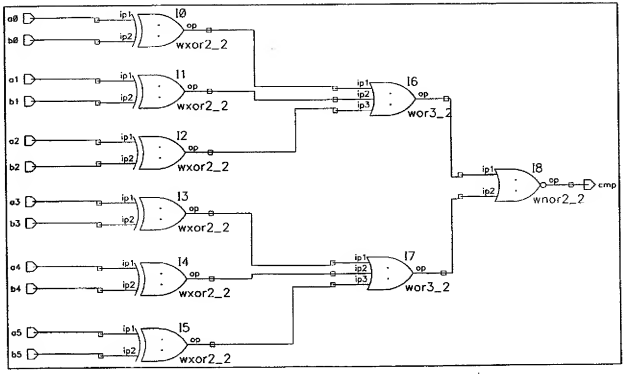

a0
b0
ip1
ip2
I0
op
wxor2_2
a1
b1
I1
a2
b2
I2
a3
b3
I3
a4
b4
I4
a5
b5
I5
ip3
I6
wor3_2
I7
I8
wnor2_2
cmp

Figure 29

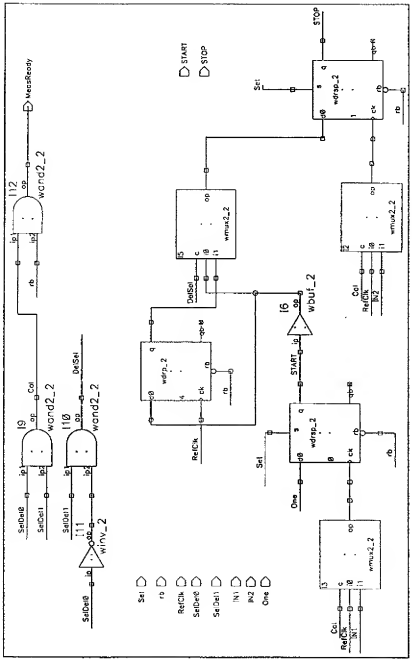

START
STOP
MessReady
wand2_2
wmux2_2
wdff_2
wbuf_2
wnot_2
SelDet0
SelDet1
DetSel
RefClk
Sel
rb
Clr
IN1
IN2
One

Figure 30

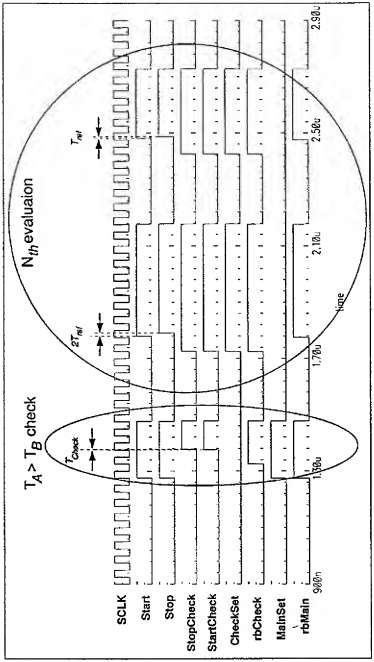

$T_A > T_B$ check
N_{th} evaluaion
T_{Check}
$2T_{ref}$
T_{ref}
SCLK
Start
Stop
StopCheck
StartCheck
CheckSet
rbCheck
MainSet
rbMain
900n
1.38u
1.78u
2.18u
2.58u
2.98u
Note

Figure 31

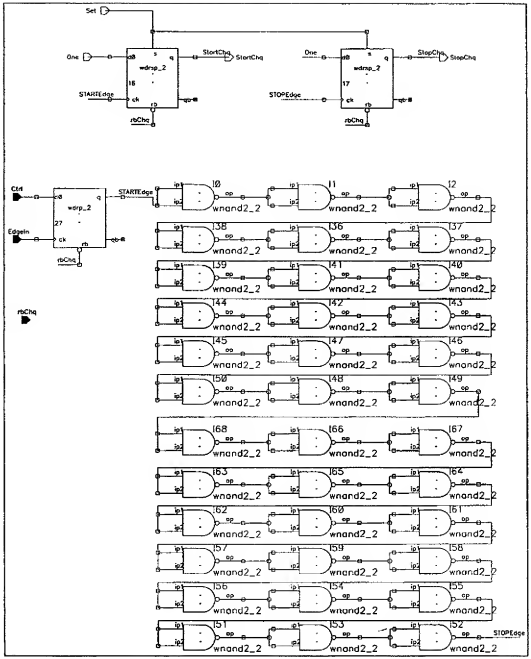

Set
One
StartChq
wdrsp_2
16
STARTEdge
clk
rb
qb
rbChq
StopChq
17
STOPEdge
Ctrl
27
Edgein
wnand2_2
STOPEdge

Figure 32